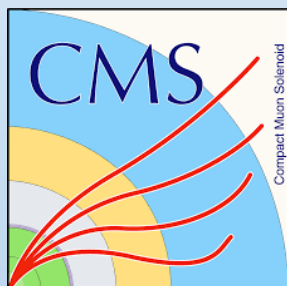
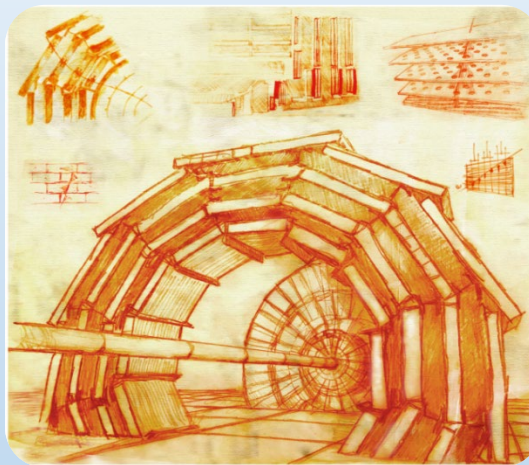


# IPM Electronics for the CMS Phase-2 Upgrade of the RPC Link System: The System Review and Validation

Wednesday Weekly Seminar



Vahid Amoozegar, Mohammad Ebrahimi, Elham Zareiyan

Behzad Boghrati, Mojtaba Mohammadi Najafabadi

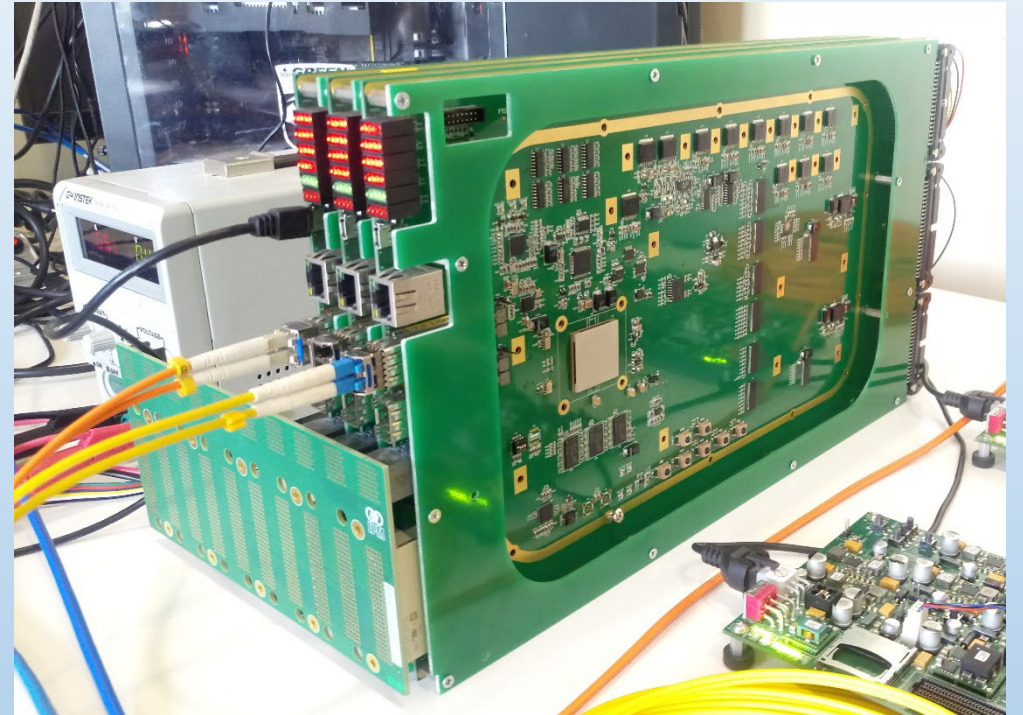
Institute for Research in Fundamental Sciences (IPM)

on behalf of Muon Group

25 January 2023

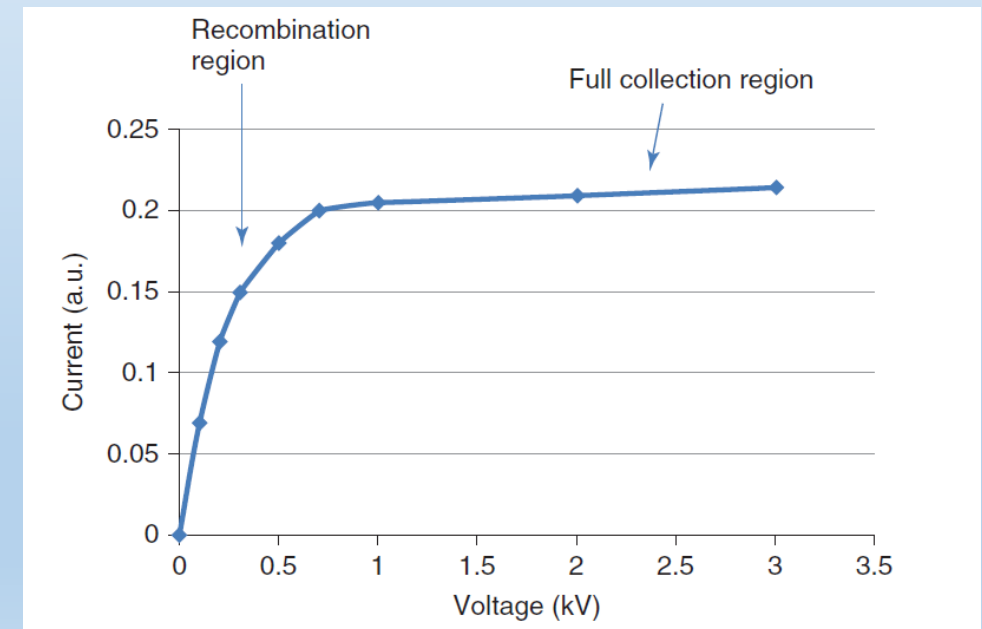
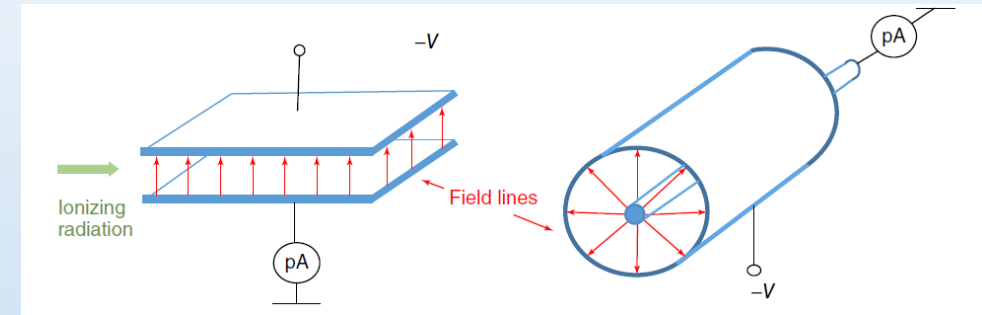


- Review on Gaseous detectors*
- RPC Detectors*
- RPC Architecture and Level-1 Trigger*
- New IPM Electronics, New Link System*
- Radiation Effects on electronics*
- Link System irradiation in CHARM*
- Summary*

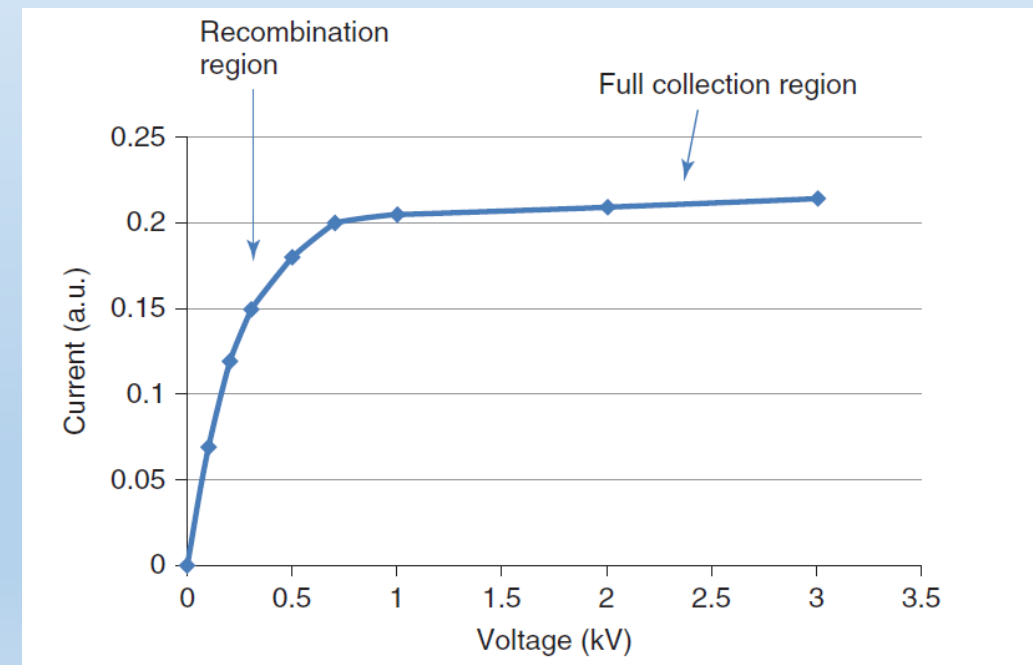
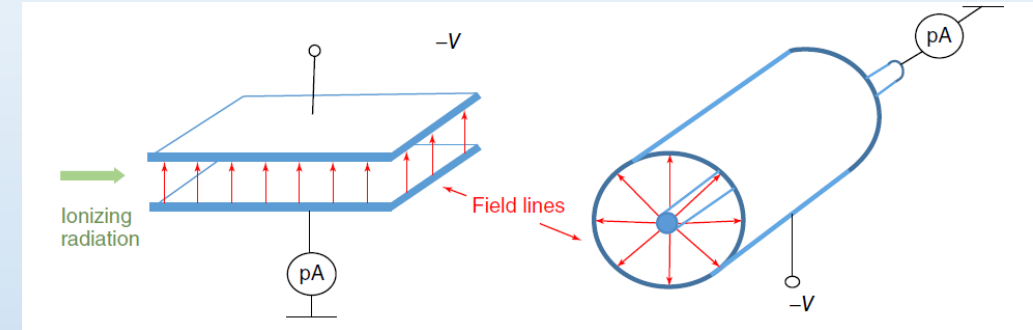


**Back-up:** *Technical Review, Radiation Effects on the Electronics,*

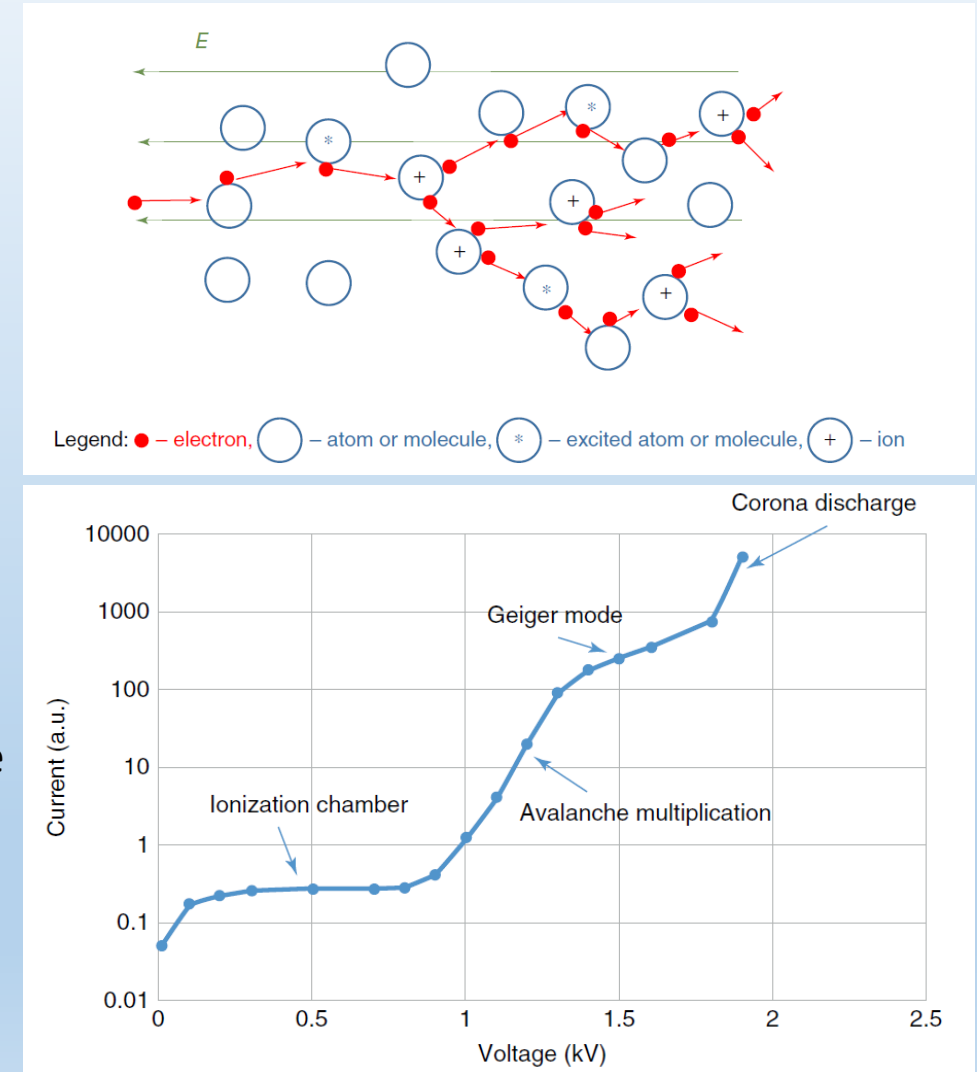
- Ionization chambers consist of two metallic electrodes: **anode** and **cathode**
- Between which an adequate voltage difference is applied.
- Such detectors can operate filled with various gases (including air), typically at a pressure around 1 atm.
- If an intense flux of ionizing radiation (either X-rays, or  $\gamma$ -rays or charged particles, which produce in the gas a certain number of ion-electron pairs) impinges in the region between the electrodes, **the resulting current, measured as a function of the applied voltage.**



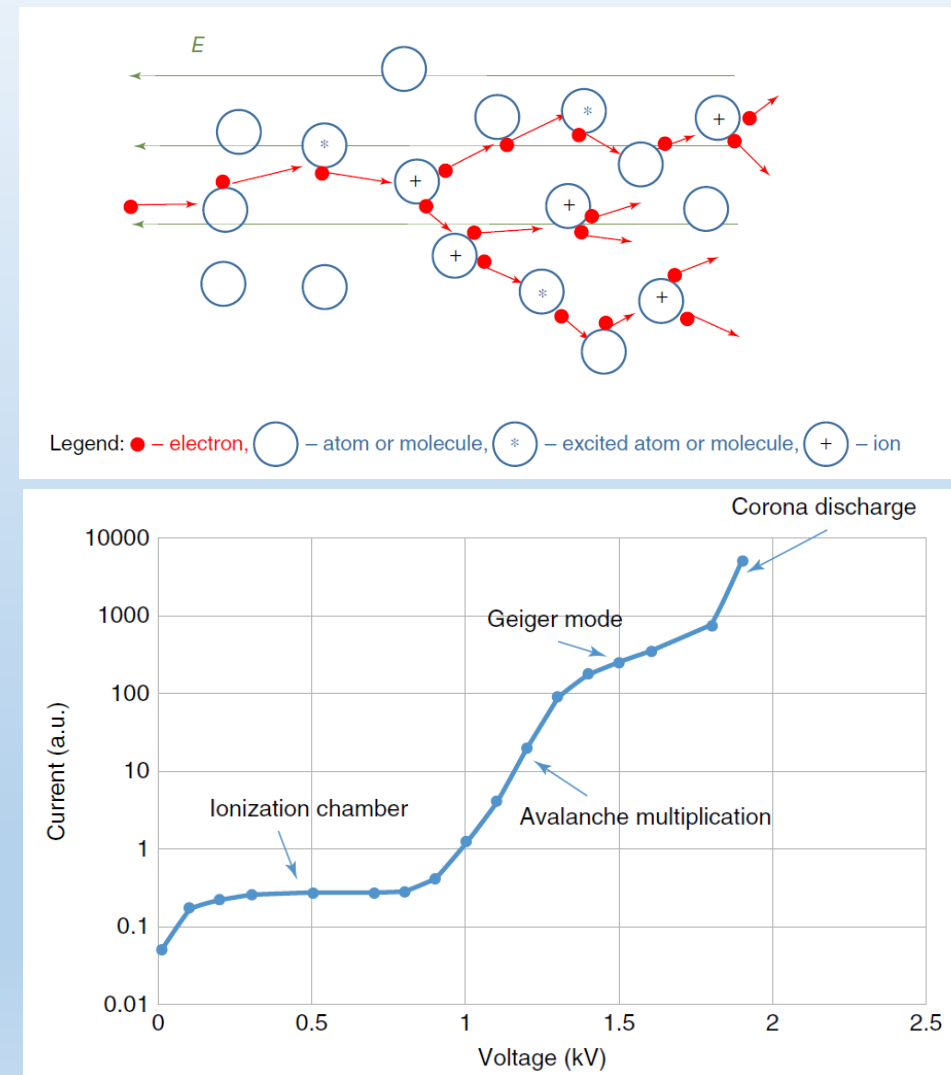
- At low voltages (roughly below 1 kV, depending on the specific geometry and gas used), it will grow until reaching a kind of **saturation region** – usually called a “plateau.”
- In this region, practically all **primary electron-ion pairs** produced by the impinging ionizing radiation are collected on the electrodes.
- At voltages below the plateau region, some electron-ion pairs **recombine**, and this is the reason why the collected current is lower than the saturated value.



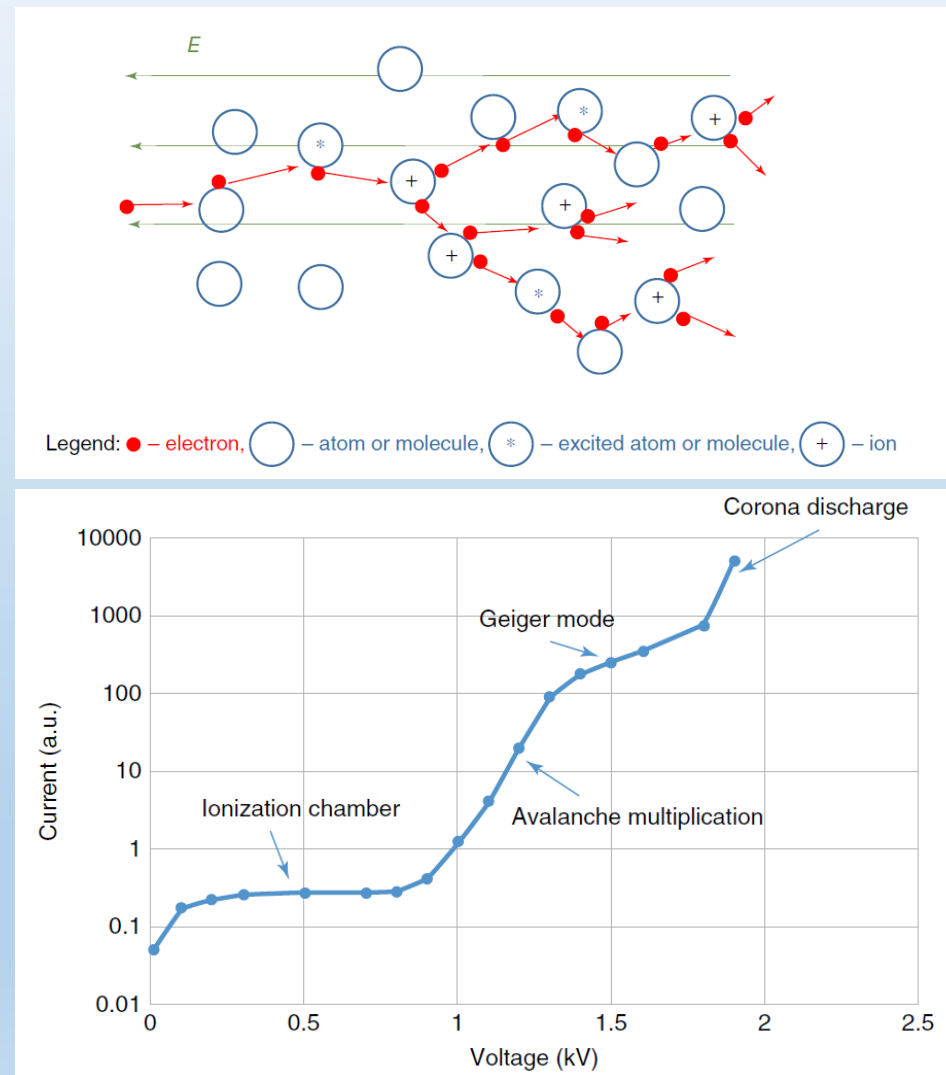
- A free electron, drifting in the gas under the influence of the electric field, experiences various types of collisions with the atoms and molecules surrounding it, which can roughly be classified into two categories:
  1. Elastic
  2. Inelastic.
- **Electron avalanche multiplication** in gases was first observed, and then carefully studied, by John **Sealy Townsend** between 1897 and 1901.
- **Electron avalanche multiplication**
- This process starts at some critical value of  $E/nA$  ( $E$  being the **electric field** strength and  $nA$  the **gas number density**, that is, the number of molecules or atoms per cubic meter), which depends on the **geometry** of the gas-filled space in which this phenomenon takes place and on the **gas** filling it.



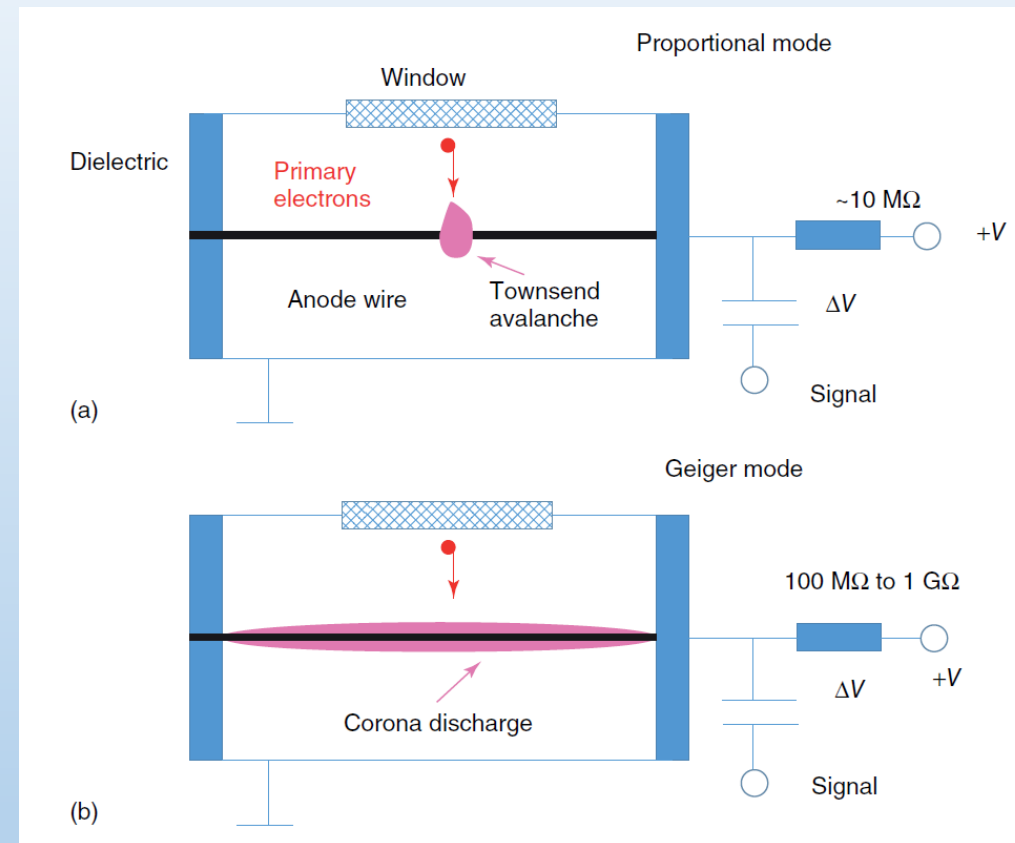
- The development of avalanches depends on their size. When this is sufficiently small, it can be safely assumed that the local electric field is almost entirely due to the external electric field (which, for instance, depends on electrode configuration, and applied voltage).
- However, it must be noted that the electric field inside an avalanche, generated by the spatial separation between the “**head**,” negatively charged, and the “**body**” of the avalanche, positively charged, is opposite in direction with respect to the external field.
- For sufficiently large avalanches, this “**space charge field**” – as it is usually called – cannot be neglected anymore, and affects avalanche development.
- **Space-charge effects**, play a very important role in the operation of some resistive detectors; in particular, when a parallel-plate configuration with quite thin (order of a few hundred micrometers) gaps are used.



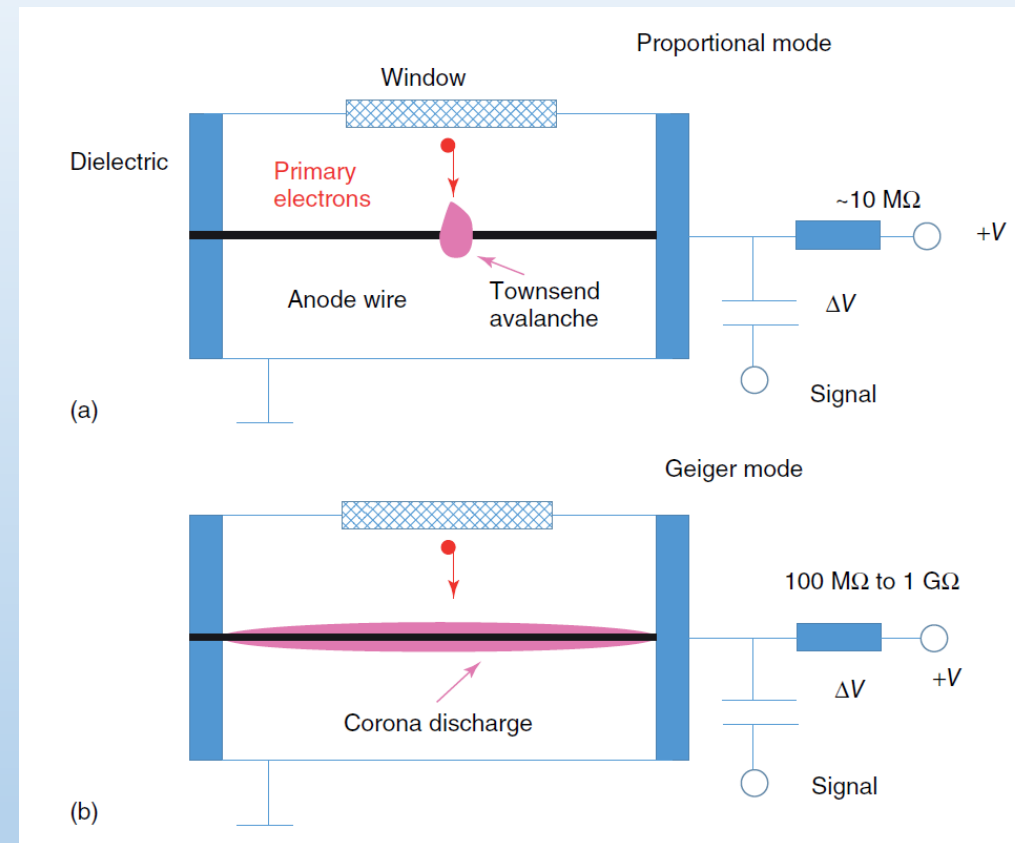
- Increasing the applied voltage beyond the **proportional region**, in the interval labeled as “**Geiger mode**”, the amplitude of all pulses from the detector becomes almost equal to each other, independent of the primary ionization  $n_0$ .
- Depending on the gas, in this region, or with another further gain increase, a **continuous discharge** called “**corona discharge**” appears.
- Geiger mode** is just an **unstable corona discharge** so there is not a clear distinction between the two operation modes.
- large resistors,  $100\text{M}\Omega$  or larger, were always used in the electric circuits of single-wire counters, connected in series with the high-voltage power supply.



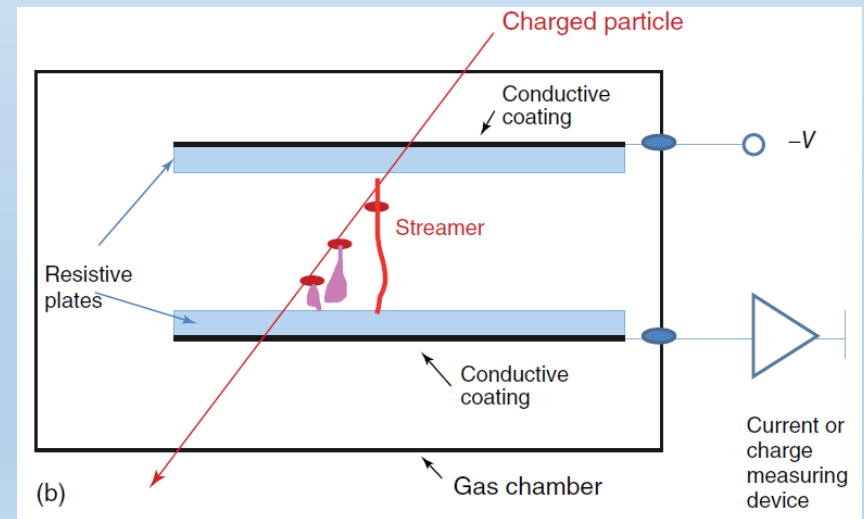
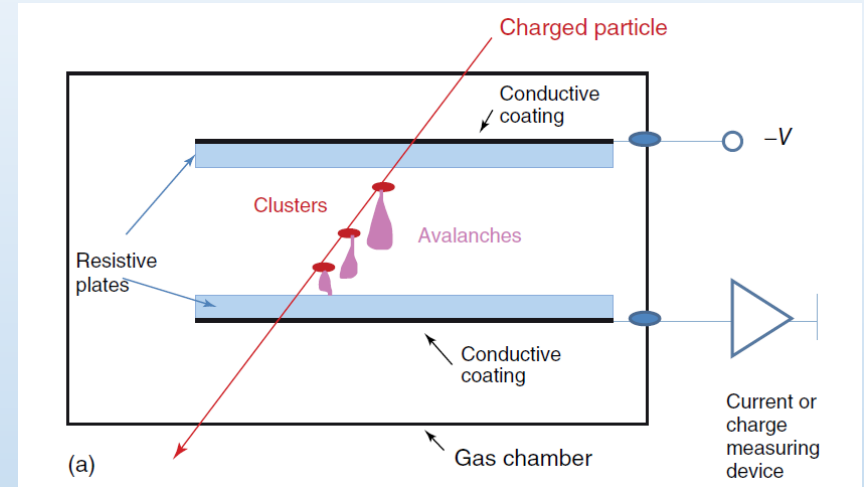
- The first gaseous detector able to record individual photons and elementary particles was the avalanche counter, invented by **Rutherford and Geiger (1908)**.
- It is a metallic cylinder (with a typical diameter of 2–3 cm) in the center of which a thin metallic wire with diameter around 0.1 mm or below is stretched.
- A positive voltage is applied to the central wire while the cylinder is connected to the ground.



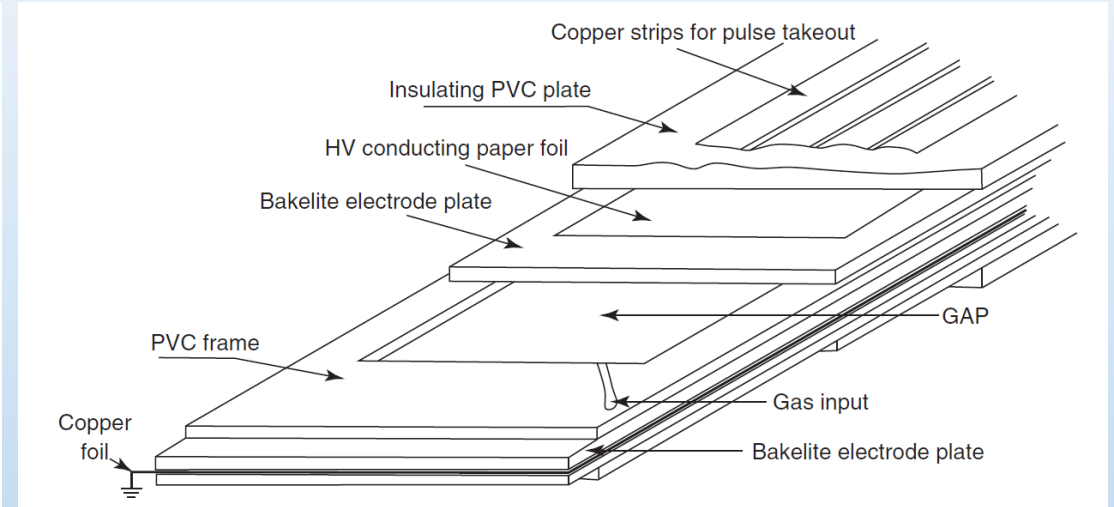
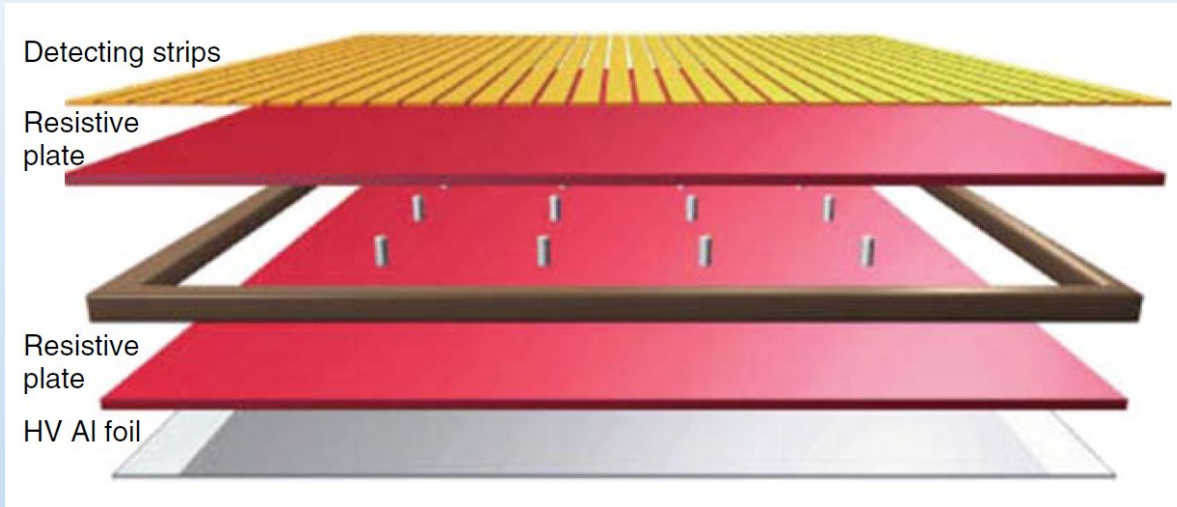
- A **corona current** (which is typically a **few microamperes**) causes a significant **voltage drop  $\Delta V$** , of even a few hundred volts, on such resistors, consequently reducing the voltage across the detector and temporarily lowering the electric field in the gas.
- As a consequence, leads to the **interruption of the corona discharge**. In this counter, the output signal is taken measuring the voltage across the **quenching resistor**; therefore, a voltage drop  $\Delta V$  of the magnitude mentioned would indicate the passage of an ionizing particle.



- As the technology in particle physics detectors progressed, new high energy physics experiments demanded not only **high spatial resolution** and **fast electronic readout** but also **better timing characteristics**.
- An interest in parallel-plate geometry detectors, offering **a minimal jitter** and thus **excellent timing**, appeared again after the invention of the so-called continuous operation spark counters (Babykin *et al.*, 1956; Parkhomchuk *et al.*, 1971).
- A very practical and successful implementation of these concepts, later on, brought about the birth of the RPCs in the 1980s (**Santonico and Cardarelli, 1981**).
- Its electrodes are not made of metal, but of materials with a relatively high electrical resistivity, typically in the  $10^{10}$ – $10^{12}$   $\Omega\cdot\text{cm}$  range, made with 1–2 mm **Bakelite** or **glass** plates.
- The outer surfaces of these electrodes are coated with a conductive or semiconductive layer to allow a reliable connection with an external applied constant high voltage.

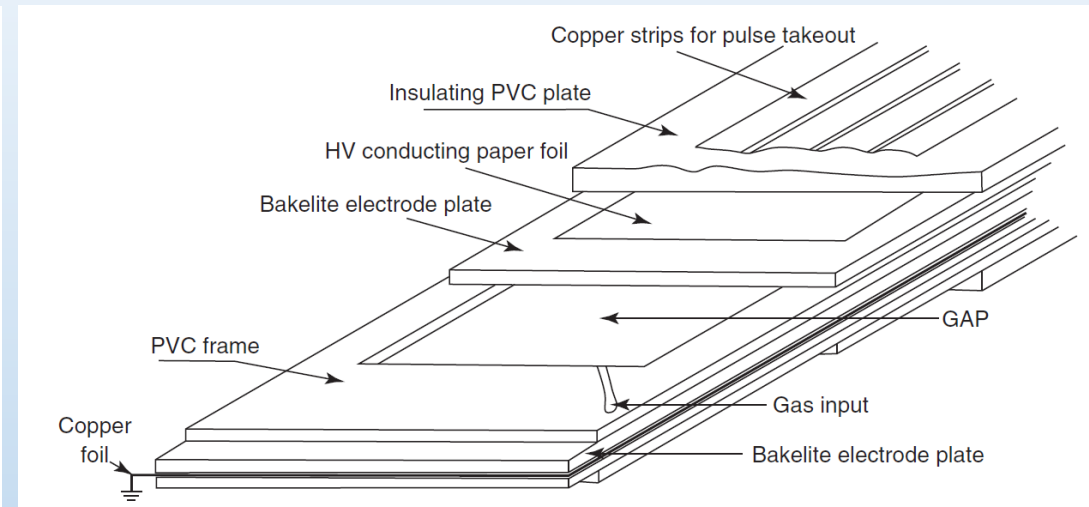
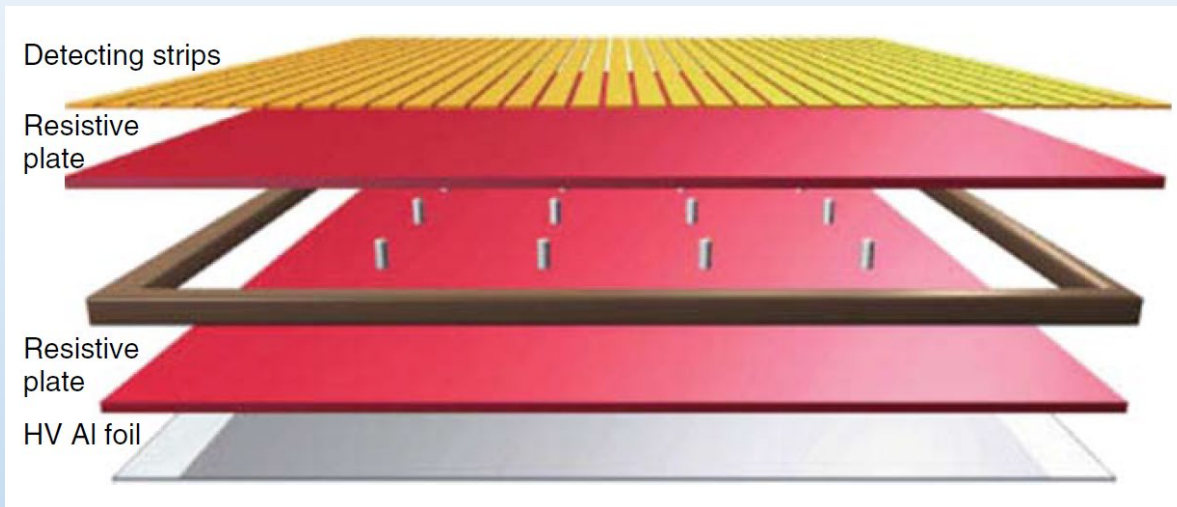






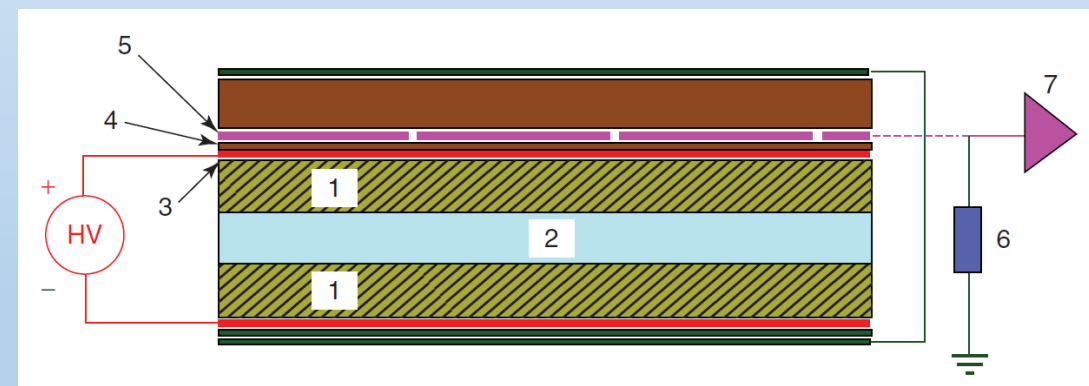
## The basic idea of the modern RPCs:

- 1) Planar geometry (with the consequent advantages of time resolution);
- 2) Use of resistive materials for the electrodes (which allowed detector self quenching and no need for a pulsed operation mode and high-voltage (HV) removal after the passage of an ionizing particle and the subsequent discharge);
- 3) Application of the HV to the electrodes via a signal-transparent resistive layer;
- 4) The idea to produce detectors that are **easy to build**, in order to make them suitable to cover large surfaces.

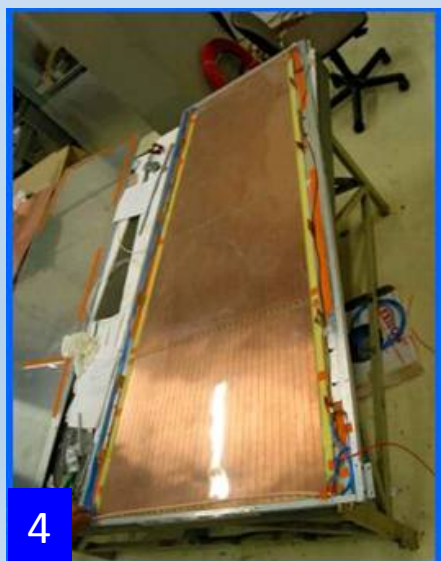


## Layout of original Santonico and Cardarelli's RPC

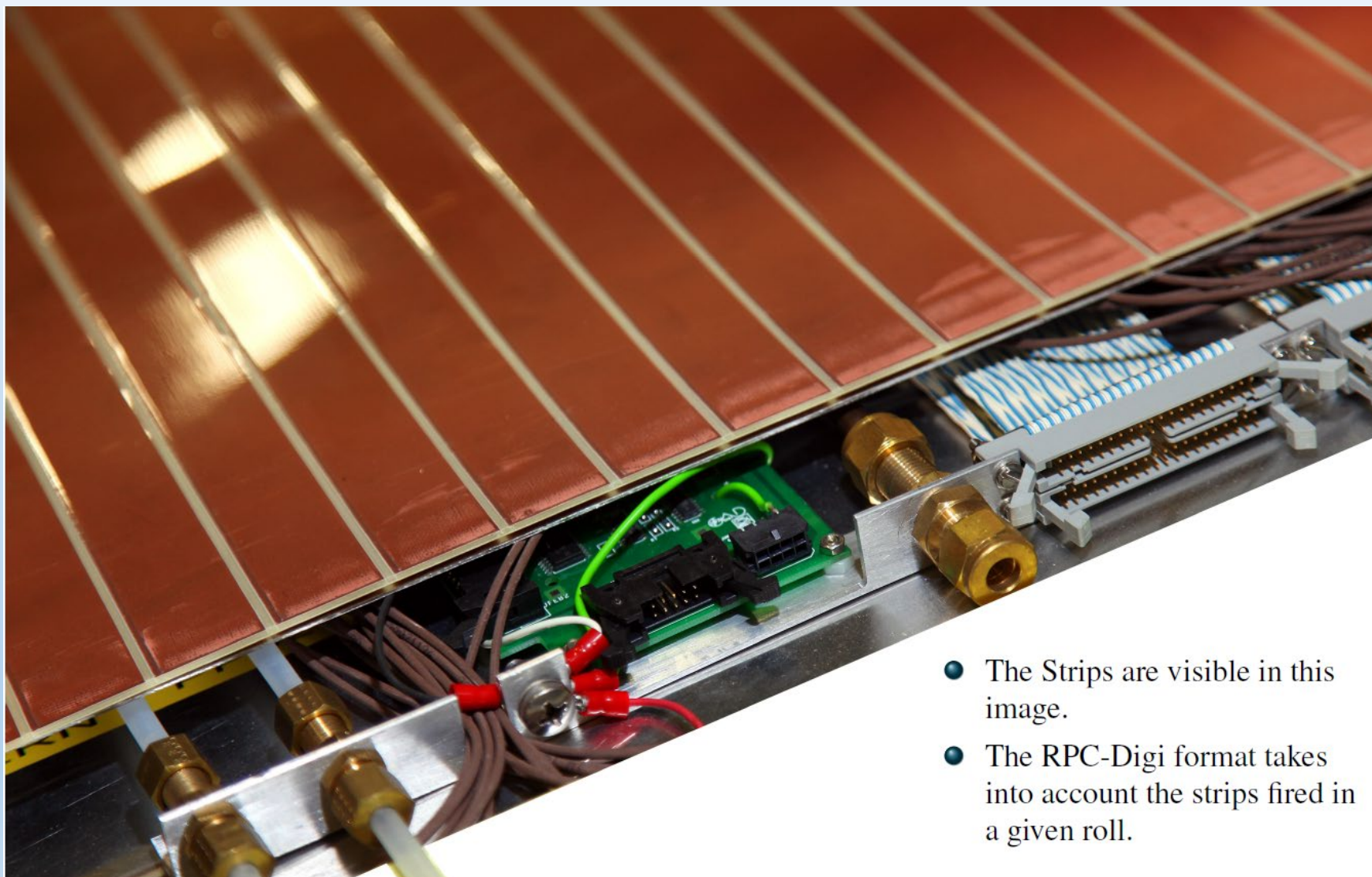
- (1) Bakelite electrodes (2 mm),
- (2) Gas gap (2 mm),
- (3) HV electrodes (200  $\mu\text{m}$  of graphite),
- (4) Mylar insulator (50  $\mu\text{m}$ ),
- (5) Readout strips,
- (6) Resistor, and
- (7) Readout electronics.



# RPC detectors - Assembling RPCs



# RPC detectors - Assembling RPCs



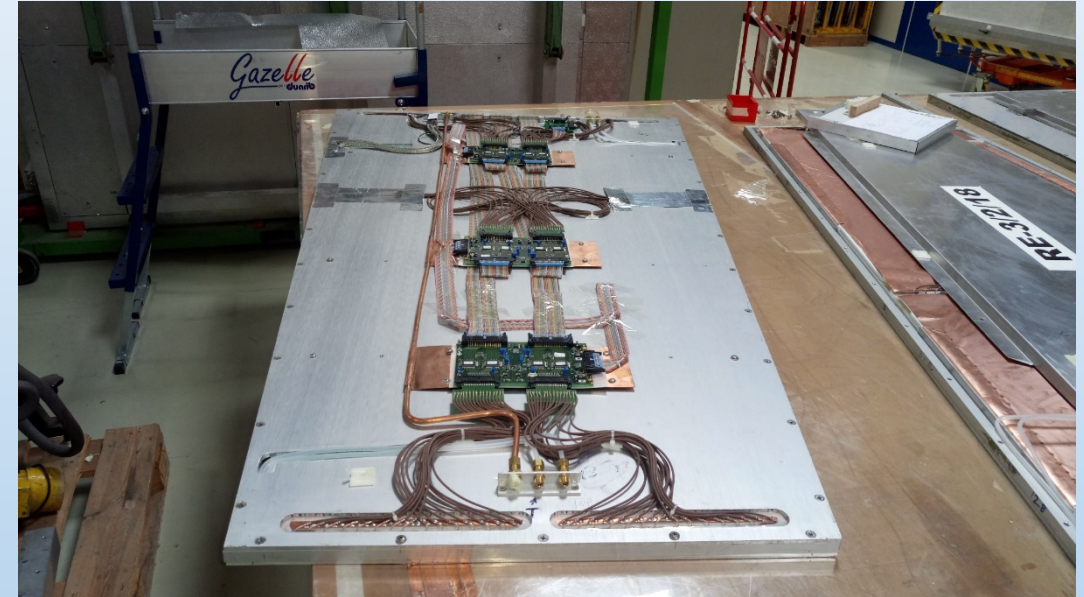
- The Strips are visible in this image.
- The RPC-Digi format takes into account the strips fired in a given roll.

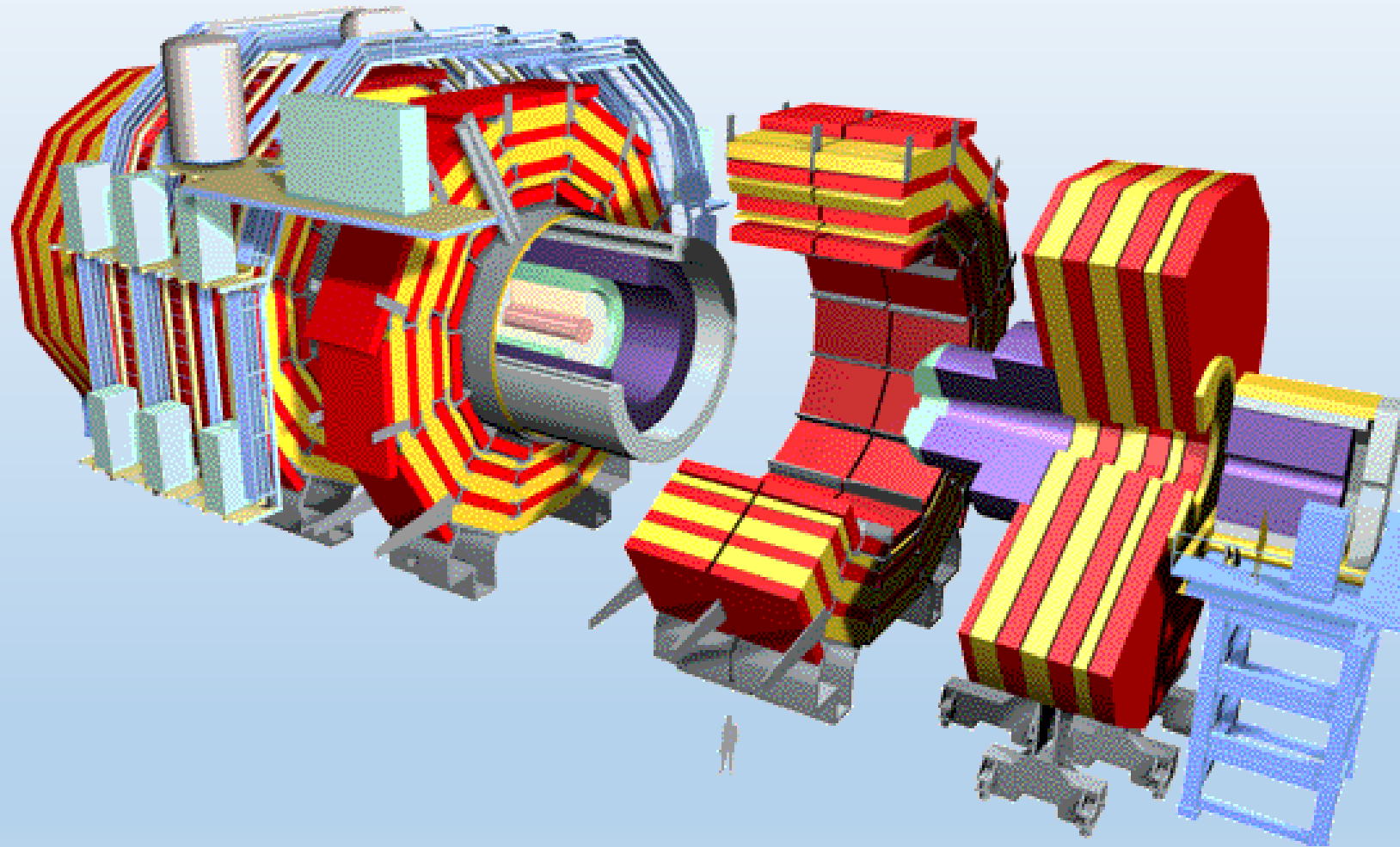
# Present RPC System Ingredients

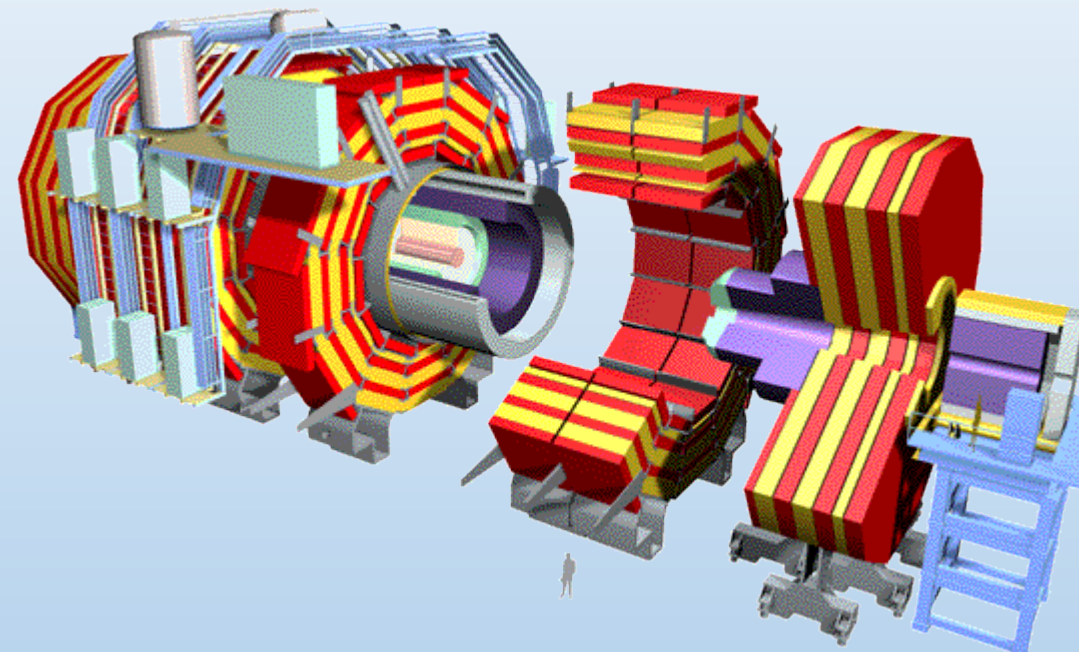


# Present RPC System Ingredients

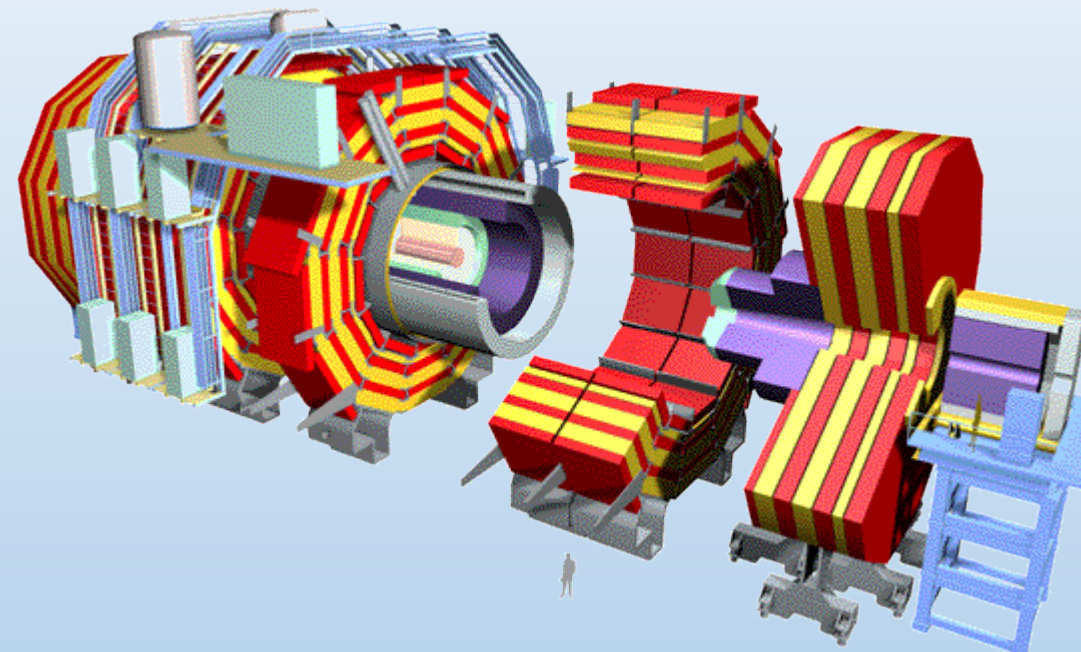
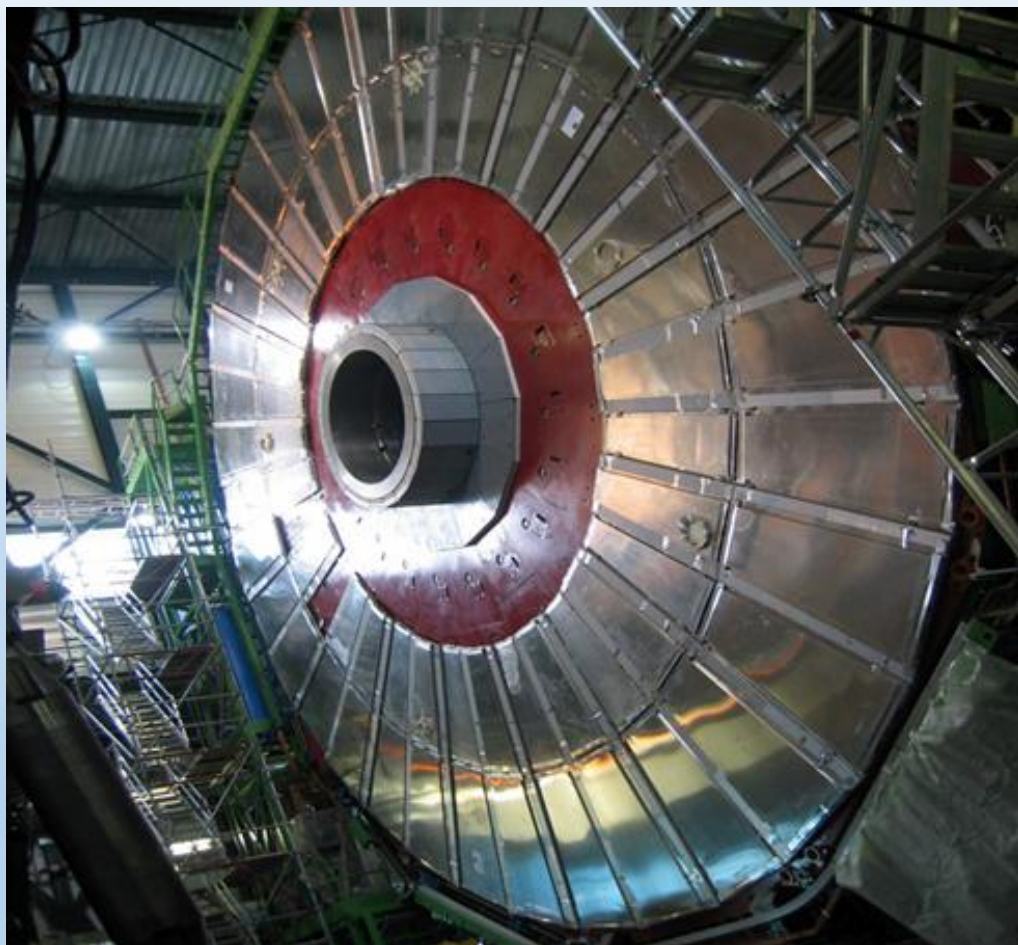
Muon subsystem	Drift Tubes (DT)	Cathode Strip Chambers (CSC)	Resistive Plate Chambers (RPC)
$ \eta $ range	0.0–1.2	0.9–2.4	0.0–1.9
Number of chambers	250	540	Barrel 480 Endcap 576
Number of layers/station	r- $\phi$ : 8; z: 4	6	2 in RB1 and RB2 1 elsewhere
Surface area of all layers	18 000 m <sup>2</sup>	7000 m <sup>2</sup>	Barrel 2300 m <sup>2</sup> Endcap 900 m <sup>2</sup>
Number of channels	172 000	Strips 266 112 Anodes 210 816	Barrel 68 136 Endcap 55 296
Spatial resolution	100 $\mu$ m	50 – 140 $\mu$ m	0.8 – 1.3 cm
Time resolution	2 ns	3 ns	1.5 ns*
Fraction of working channels	98.4%	99.0%	98.3%







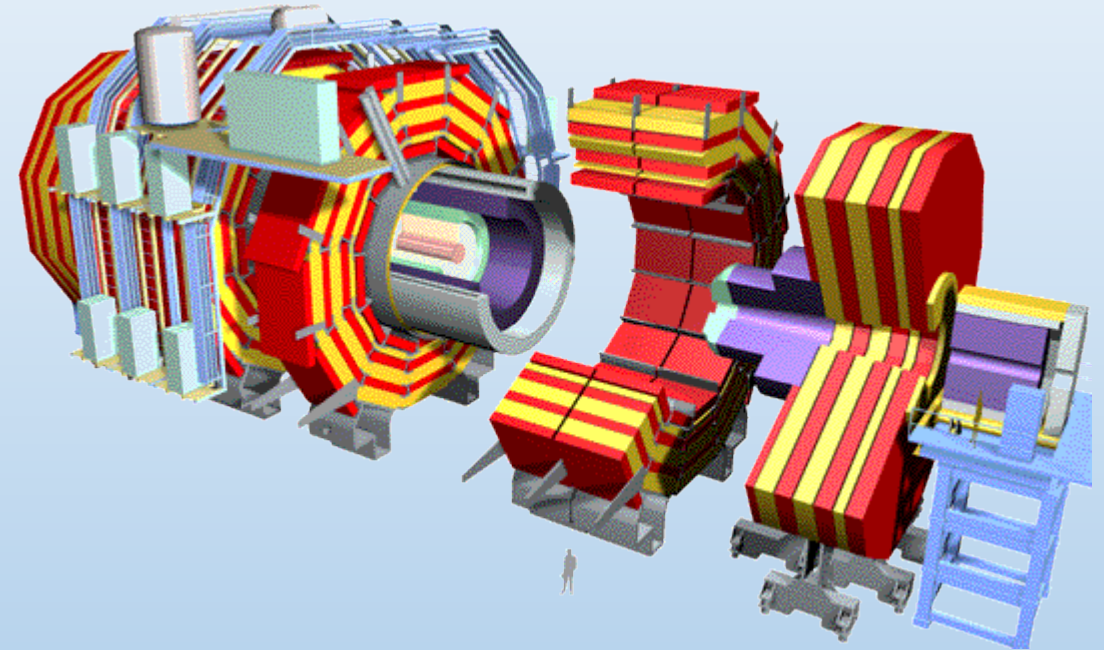
- **Iron yoke layers**
- **Ring:** In the barrel the ring could be -2,1,0,1,2 referring to each wheel in the barrel system.

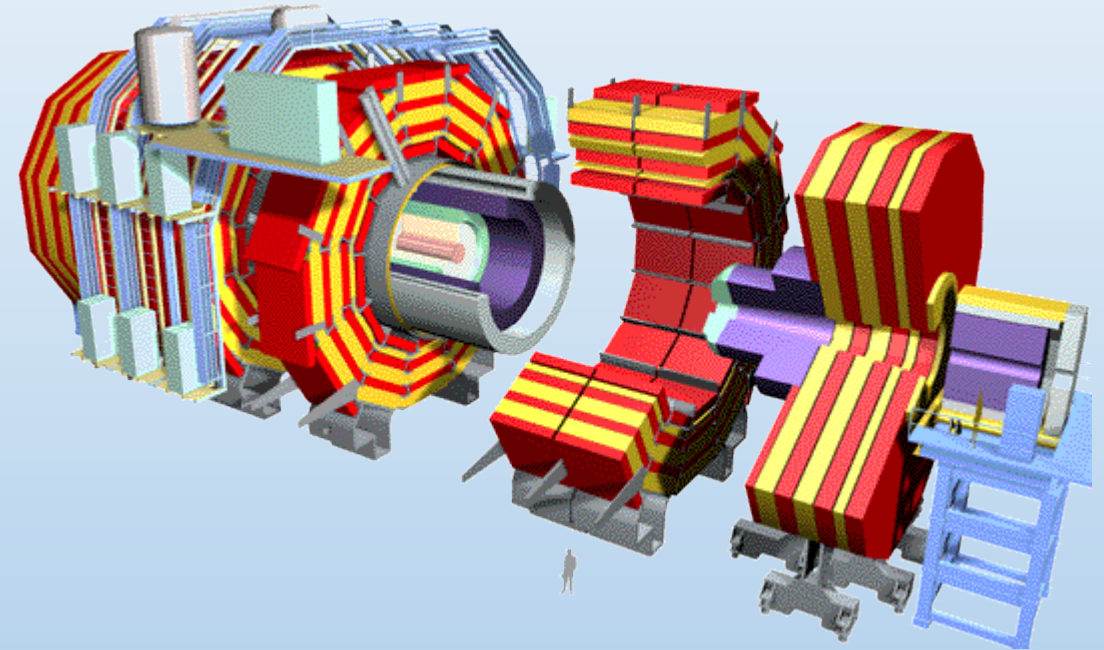
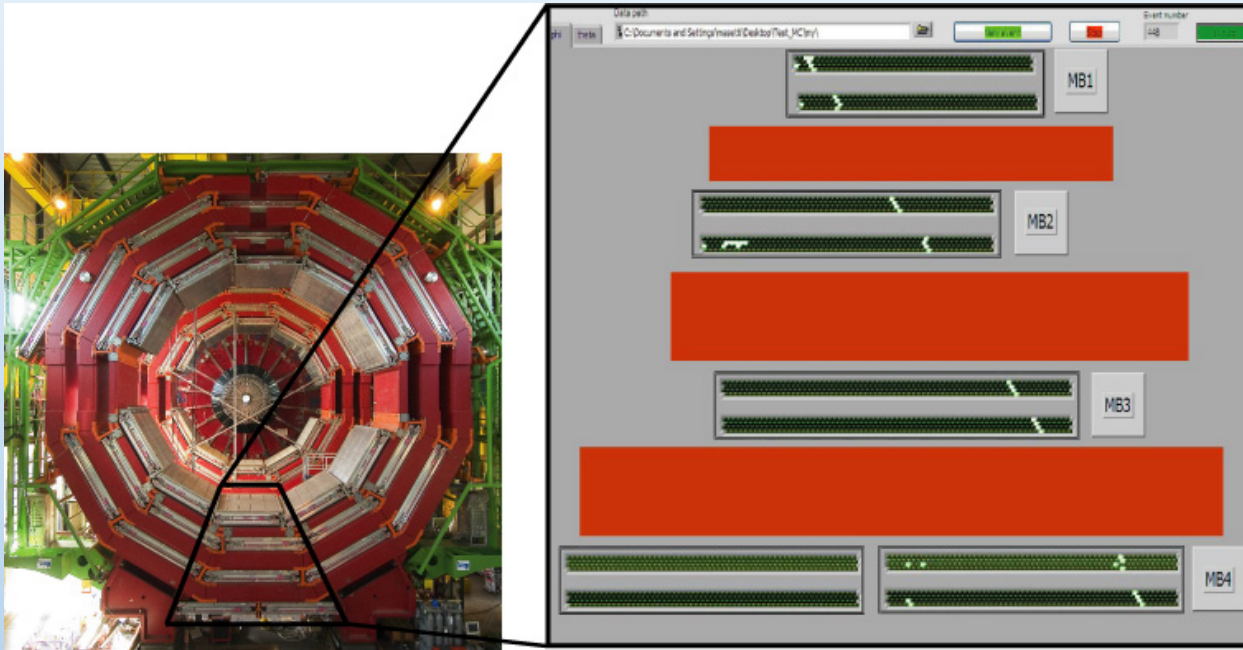


**Disk:** In the Endcap, with rings 2 and 3 installed and with the space devoted for the ring 1.

## Station:

1. In the Barrel the stations could be 1,2,3,4 they are shown in the yellow part of the following plot. And represent each cavity in between the iron yoke layers.
2. In the Endcap there are just 4 stations 1,2,3,4 they represent the disk.





## Sector:

1. There are 12 sectors in the barrel, sector 10 is show in the image below.
2. One wheel has 12 sectors

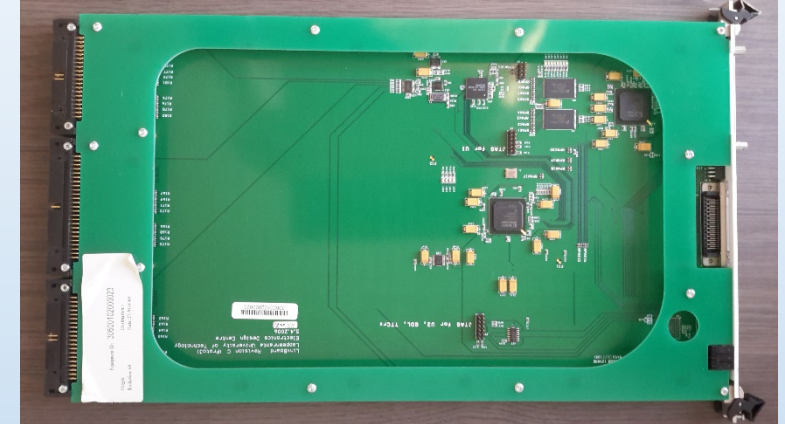
# Present RPC System Ingredients



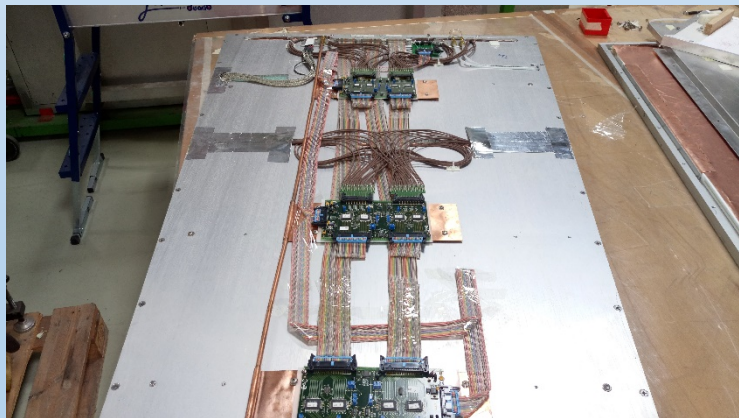
**RPC Endcap Chamber**



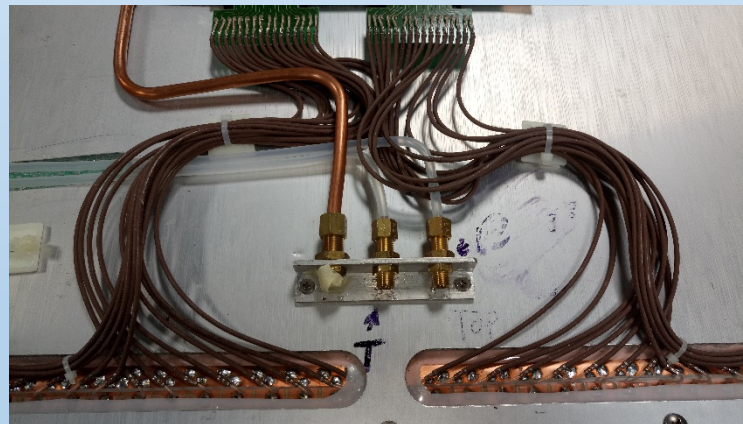
**Front-end Board**



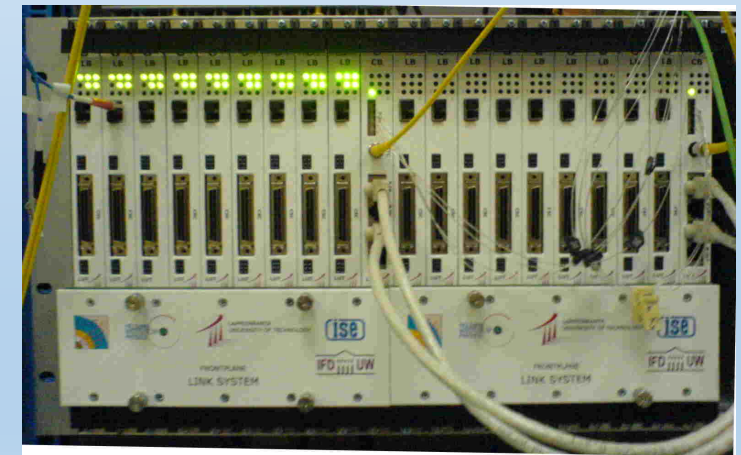
**Link Board**



**On-detector Electronics**

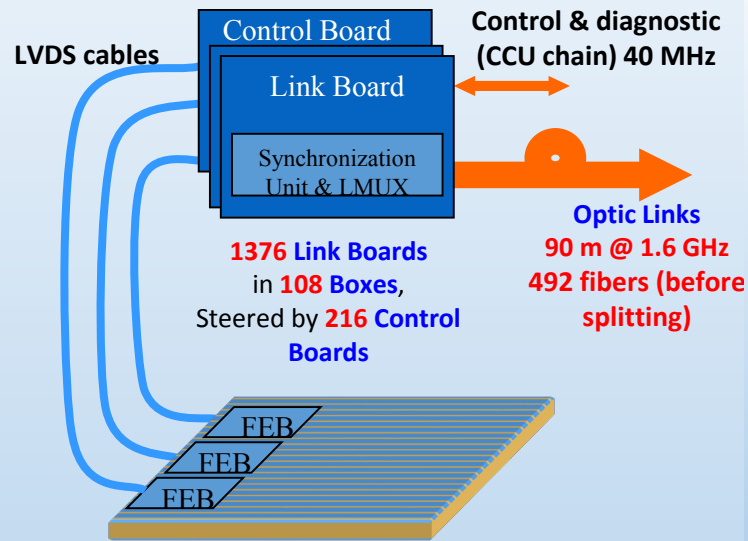


**RPC Strips, Coaxial cables,  
Cooling and Gas Pipe**



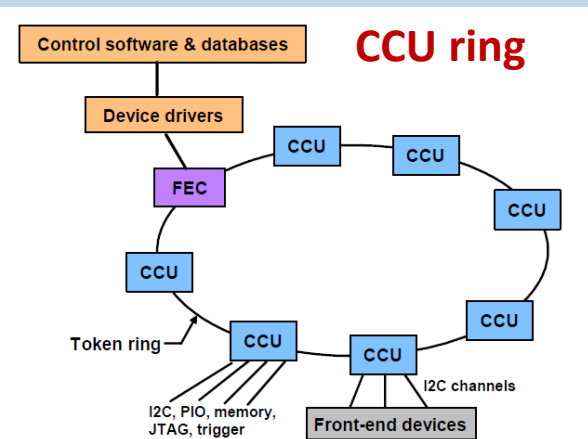
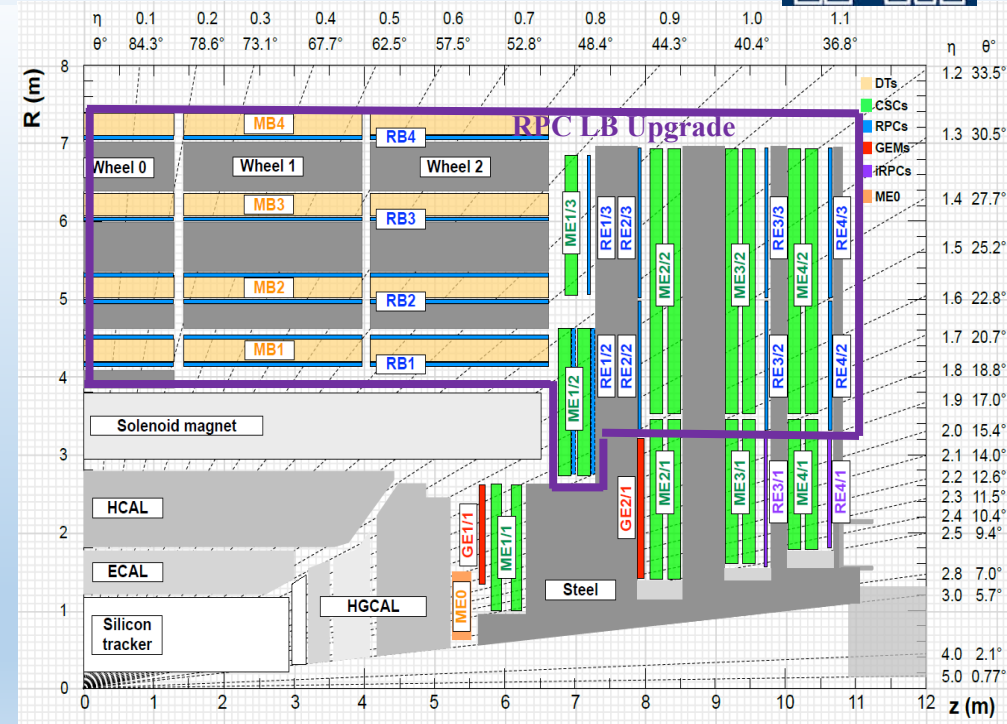
**Link System**

## Present RPC Link System



## Upgrade Motivation

- RPC signals synchronization, **timing resolution is 25ns**
- Data transmission speed is about **1.6 Gbps**
- Control, diagnostic and monitoring of the Link system has been designed based on **CCU ring** (combination of copper cable and fiber optic), very susceptible to electromagnetic interference



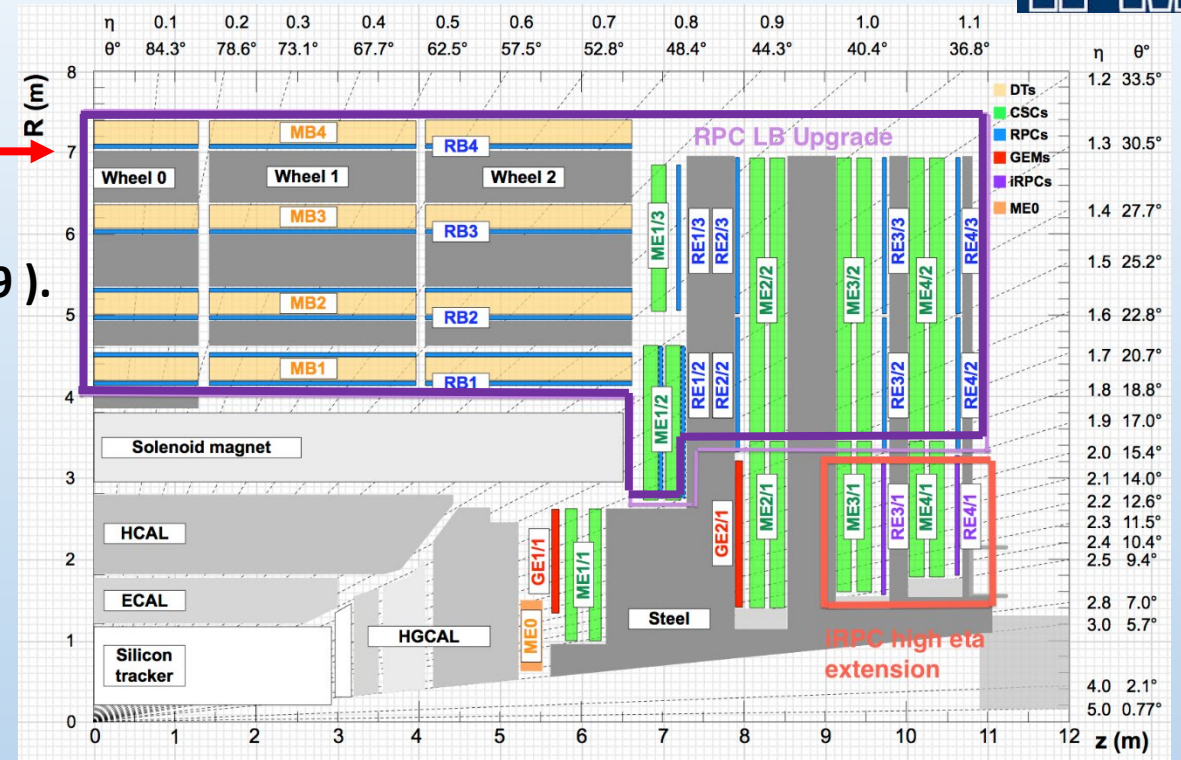
- CCU ring is not very fast, the bandwidth (40 MHz) share between 12 control boards
- Most radiation hard electronic components are obsolete
- Electronic aging, presently the Link system at the **end of LS2** is already **13 years old**



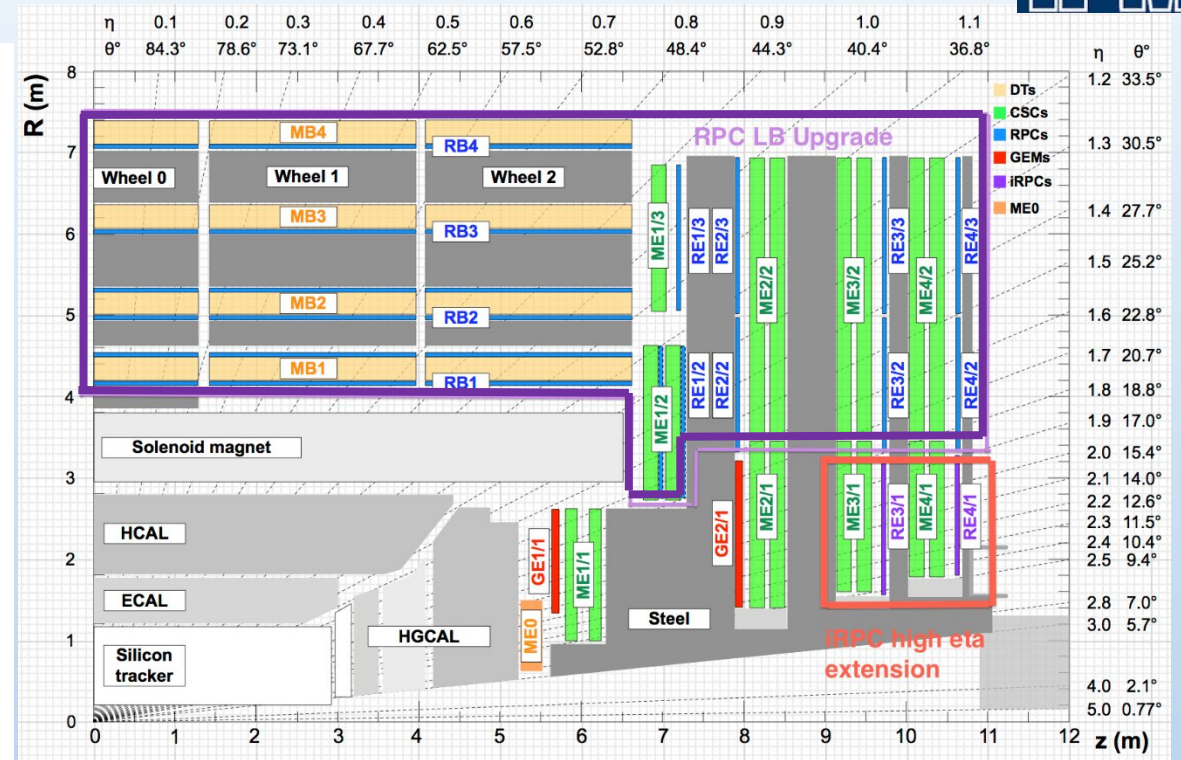
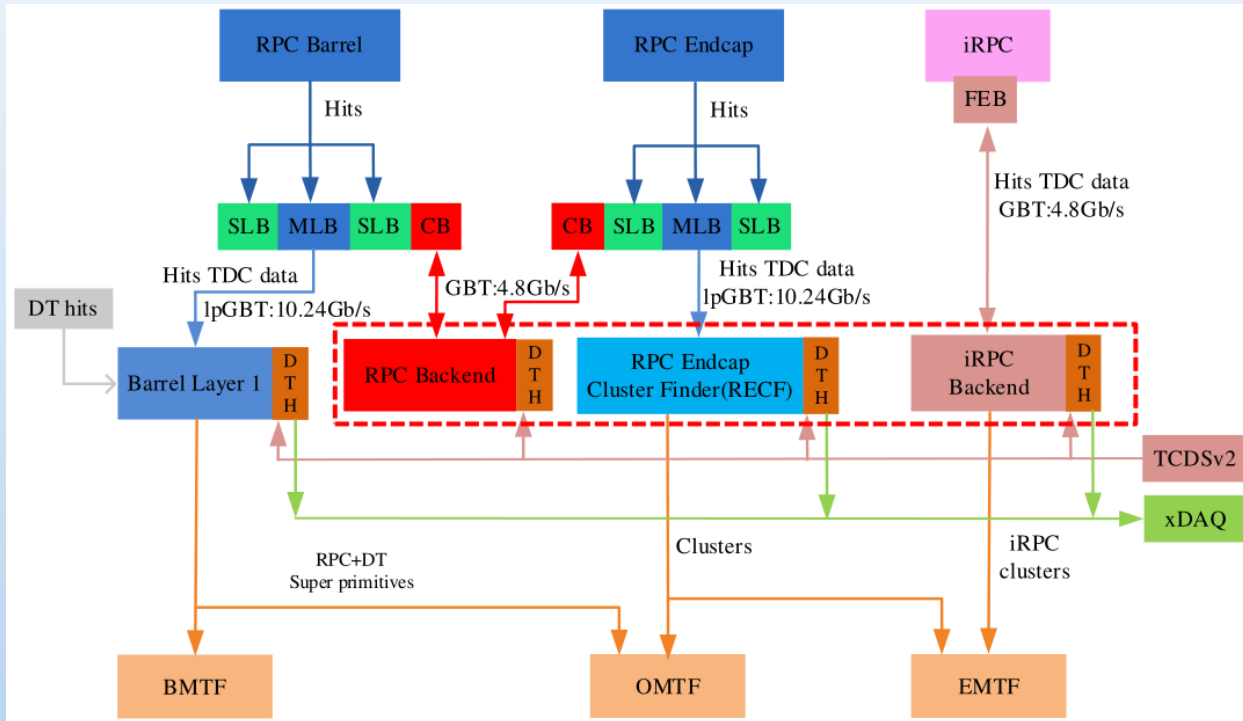
# RPC Phase-2 Upgrade Project for HL-LHC

## Present RPC Upgrade Project scope

- New electronics for the legacy detectors.
- Replace all off-chamber electronics.
- To improve timing resolution for existing RPC ( $|\eta| < 1.9$ ).
- Ready for installation in EYETS 2024/2025.



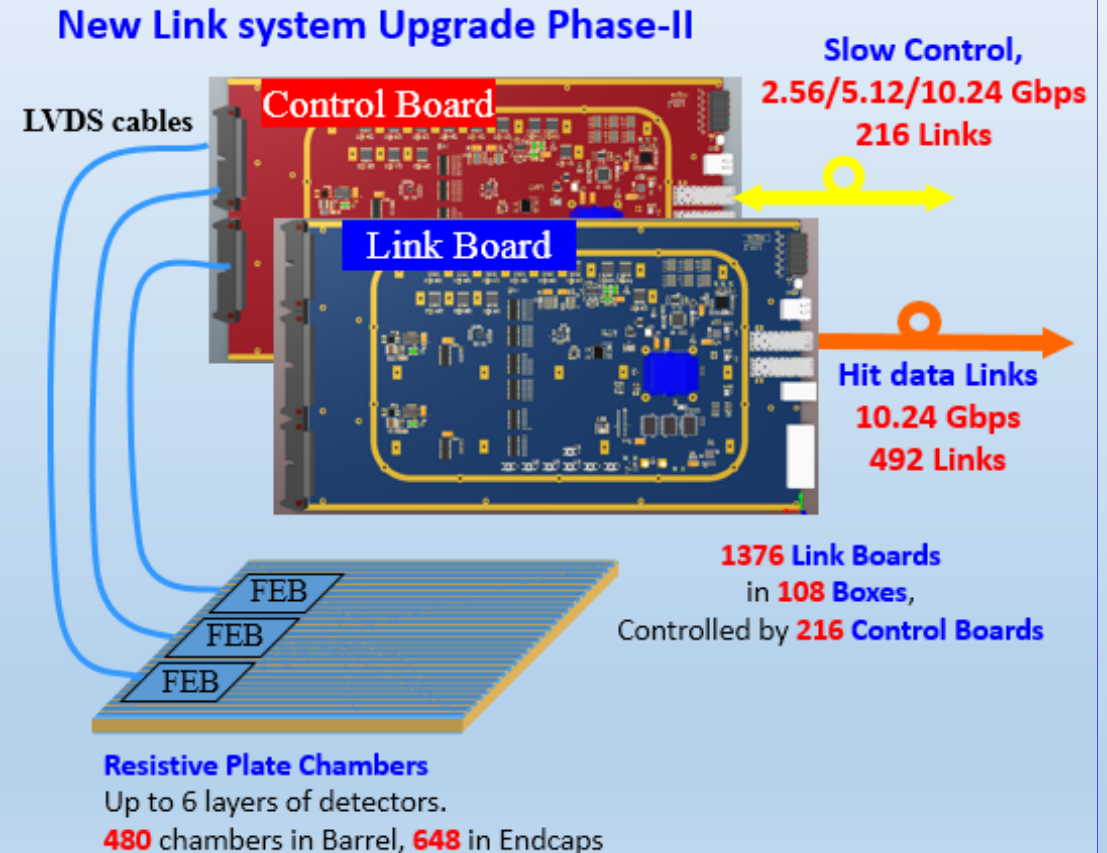
# RPC Phase-2 Upgrade Architecture and Layer1



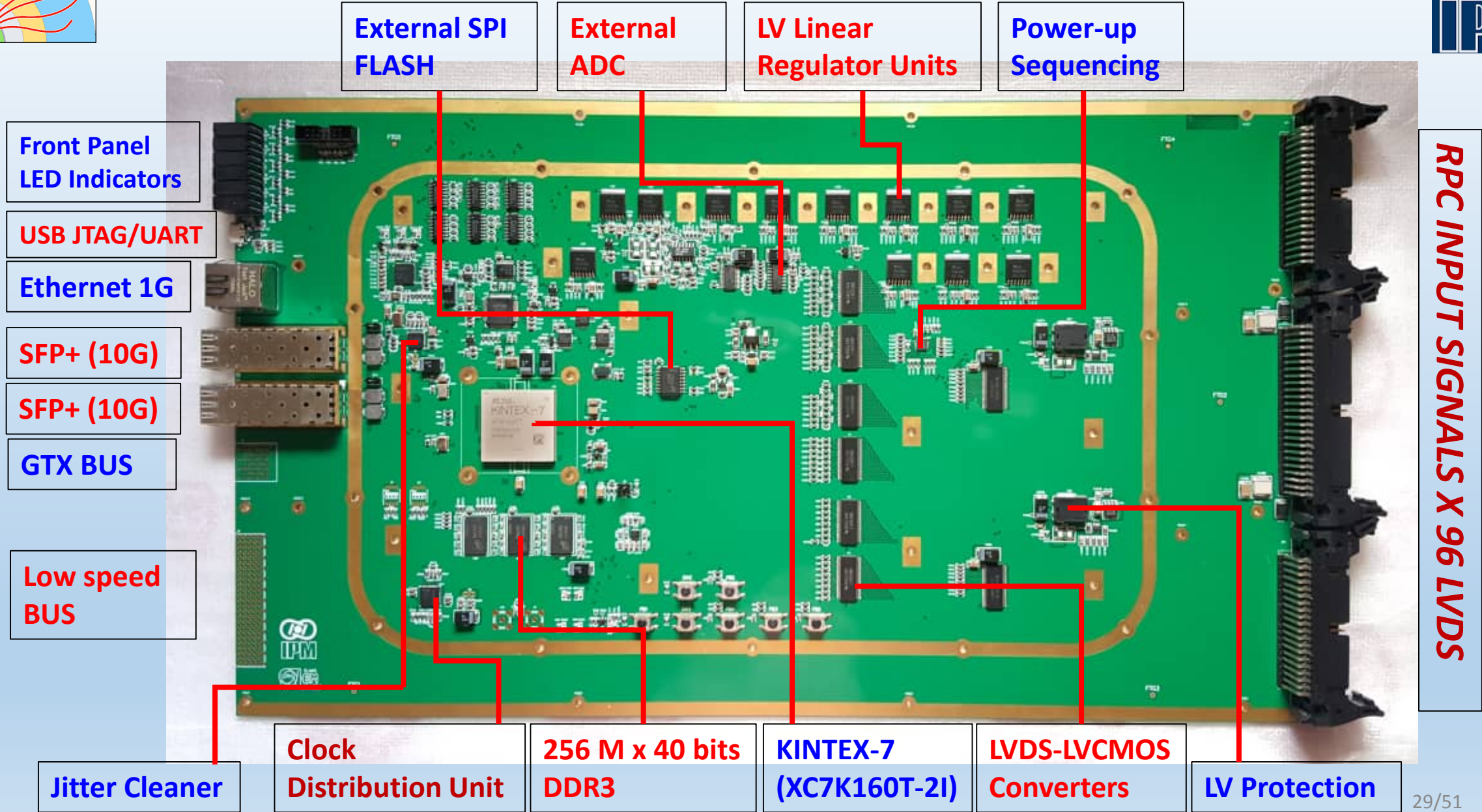
- SLB:** Slave Link Board
- MLB:** Master Link Board
- CB:** Control Board
- B/O/E MTF:** Barrel/ Overlap/ Endcap Muon Track Finder

## New Link system Features :

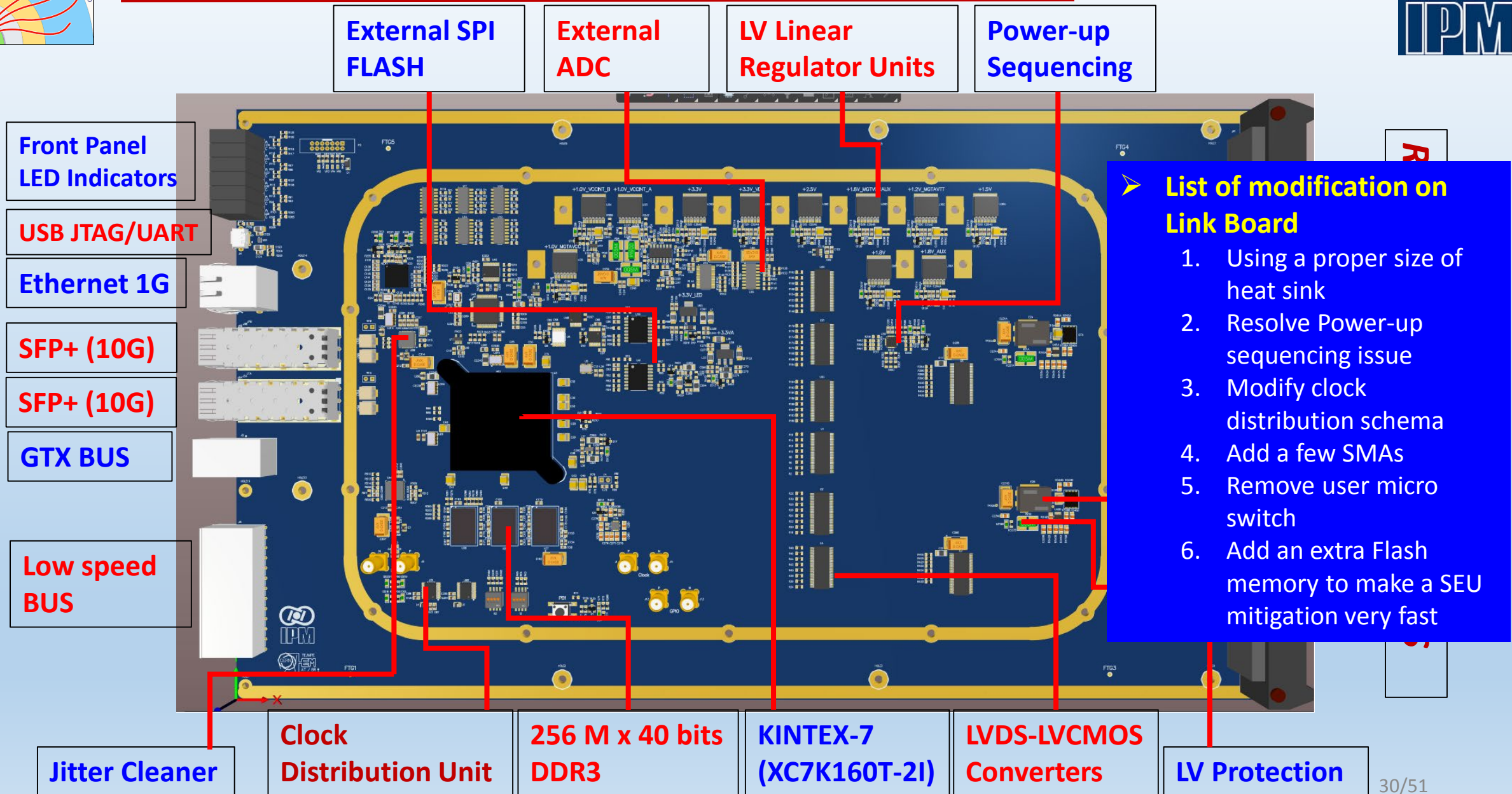
1. 14 Layer PCB ,  $40 \times 28 \text{ cm}^2$
2. FPGAs are **KINTEX-7, XC7K160T – Industrial Version**
3. Muon hit time, TDC timing Resolution : **1.56 ns**
4. Master Link board output data rate : **10.24 Gbps**
5. Control Board communication with RPC Backend electronics: **4.8 Gbps**
6. Input Voltage: **4.0 V (3.8V – 5.1 V)**
7. Current: **3 A -> 2 A**
8. Power Consumption: **12 W -> 8 W**
5. Embedded internal buffer (DDR3) : **4 Gbyte**
6. Optical Transceiver: **SFP-10G-SR**
7. Radiation Mitigation: **TMR + Internal Scrubbing**
  - Scrub Rate of entire FPGA (Real time SEU detection and Correction) : **13ms** (31,770 times faster than the rate of SEU at the tower racks)
  - SEU at the tower racks : **Every 413000 ms**
8. Safety Systems:
  - Over & Under Voltage Protection, FPGA Over temperature Protection, Transient Voltage Suppressor
  - ESD Protection (15 kV)



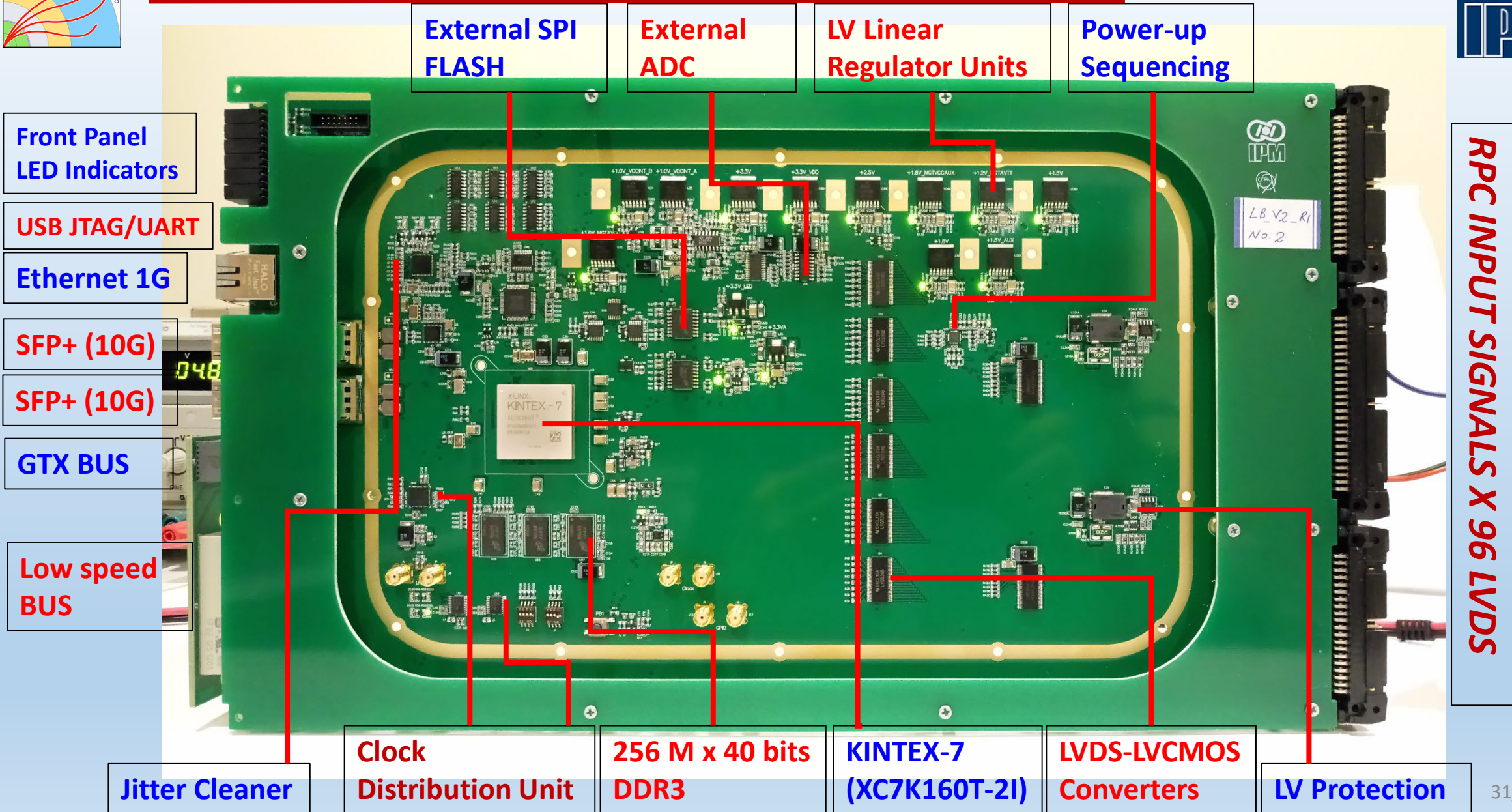
# Hardware Prototype of New Link Board(V2.r0)



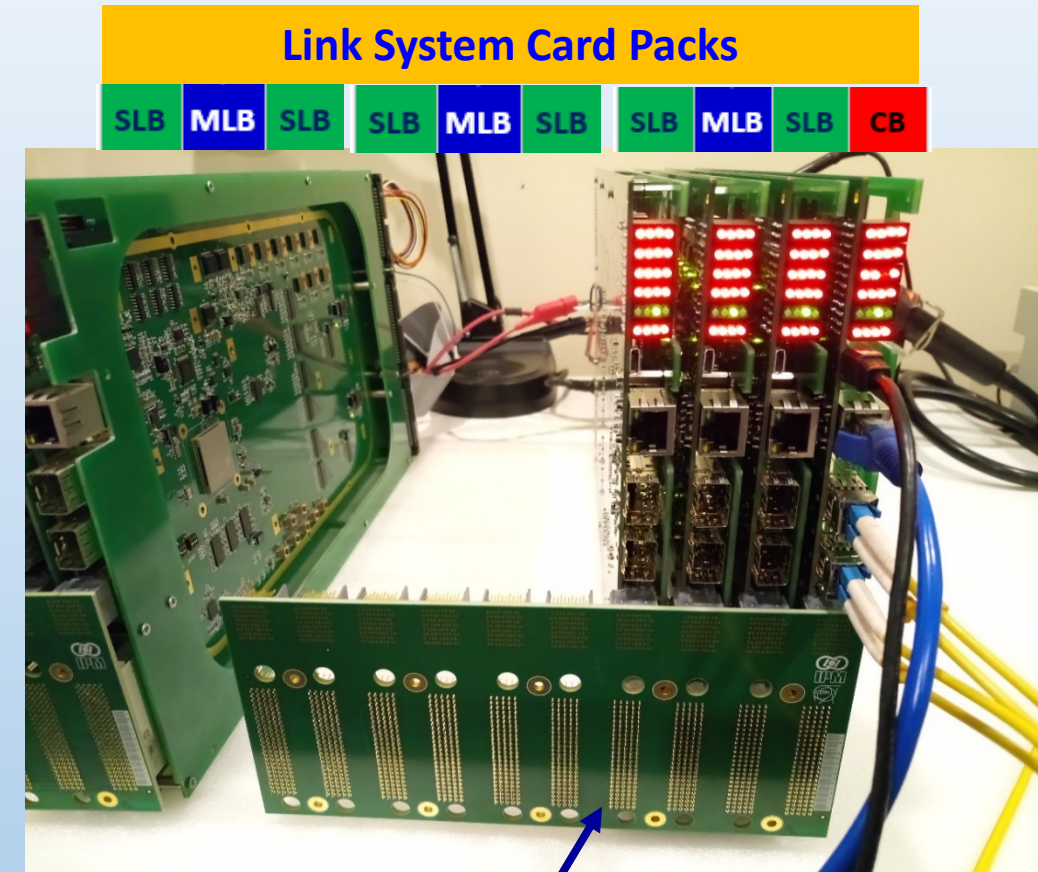
# Hardware Prototype of New Link Board (V2.r1)



# Hardware Prototype of New Link Board (V2.r1)



1. **Signal Conditioning:** Single LVDS signal (pair of wires/pins) for each RPC channel (strip). RPC hit is a pulse of 100ns.
    - Each LB receives 96 RPC channels i.e. full Endcap RPC (3 eta rolls),
    - or one roll of barrel RPC.
  2. **Impedance Matching:** According to the LVDS standard, the line should be terminated on the receiver side by  $\sim 100 \Omega$  resistance inside the LVDS line receiver chips.
  3. **Time-Stamping:** The signals are asynchronous, and the rising pulse edge brings information about the RPC hits timing (the signals are not synchronous to any clock). Time-Stamping unit, implemented in the FPGA, measures the arrival time of the rising edge of the pulses to the corresponding bunch crossing.
  4. **Latency Compensation:** The RPC signal and received TTC clock has been delayed concerning the main bunch crossing and should be fixed first. RPC signal delay and TTC clock phase shift compensator.
  5. **Data collection and transmitter:** Data of 42 fired strips at each bunch crossing are selected and buffered by the data collector inside the Link Board FPGA. Crossing data of 6 hits from one Link Board will be sent to the Master Link Board. In the Master Link board, its data and the data of two adjacent Link boards are collected and merged. At Final, data of 18 hits of current bunch crossing will send to the next layer of the trigger.
- **Master/ Slave Link Board:** The system is built with Slave Link Boards and Master Link Boards, the PCB is the same, but the firmware is different.

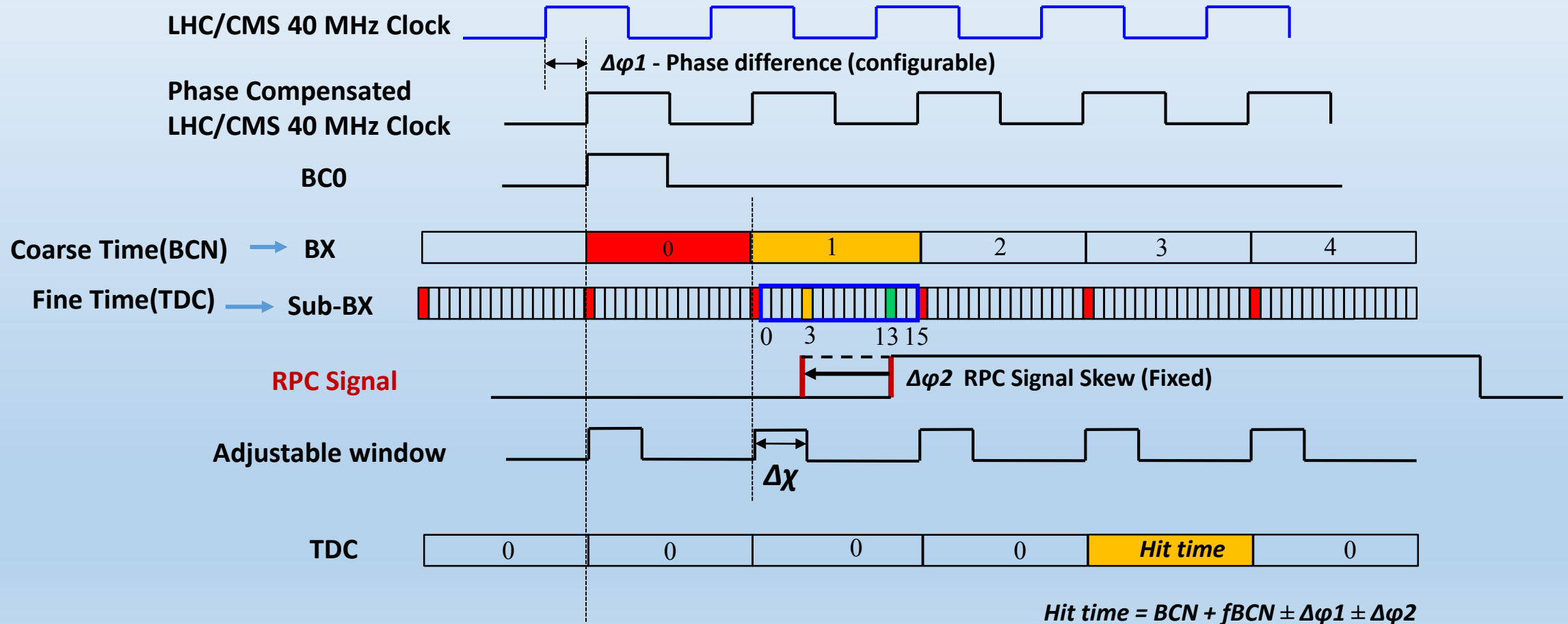


- Link System Front Panel
- 16 Layer PCB
- Board will be cover by an insulator layer

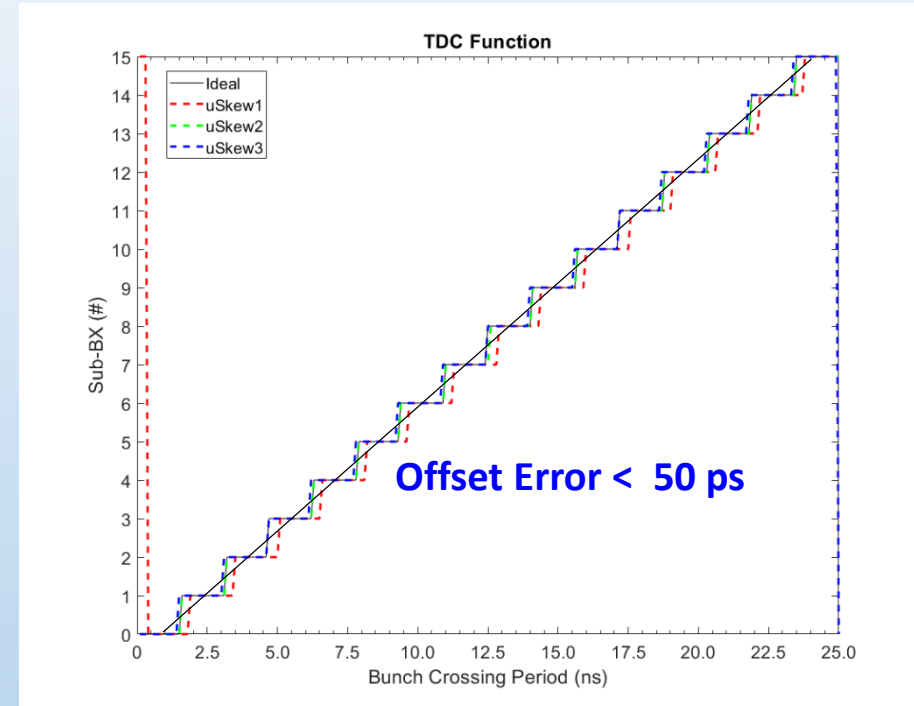
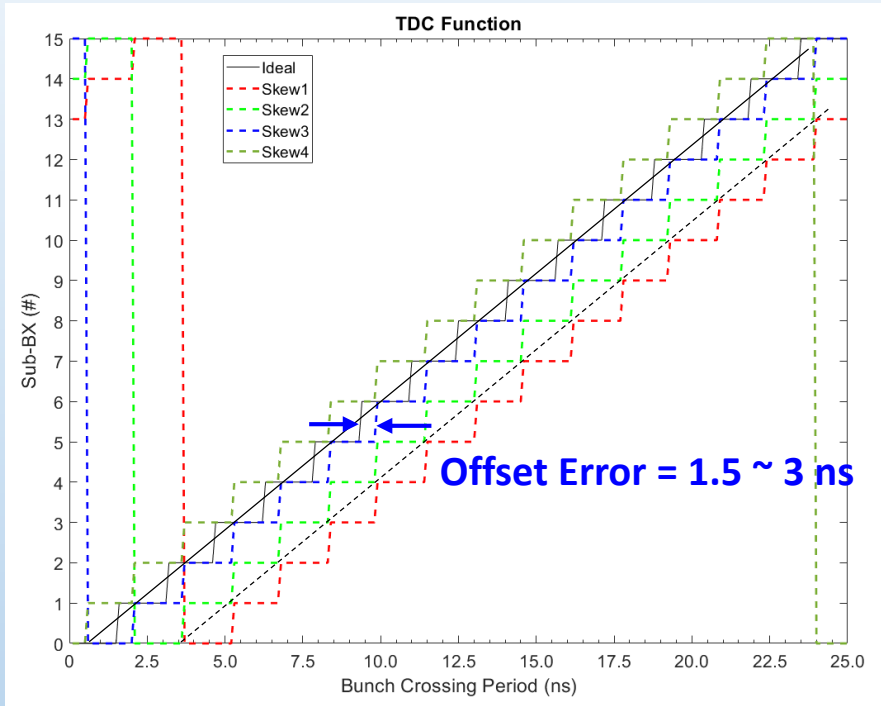
# Time-Stamping

- **RPC signals time Stamp**

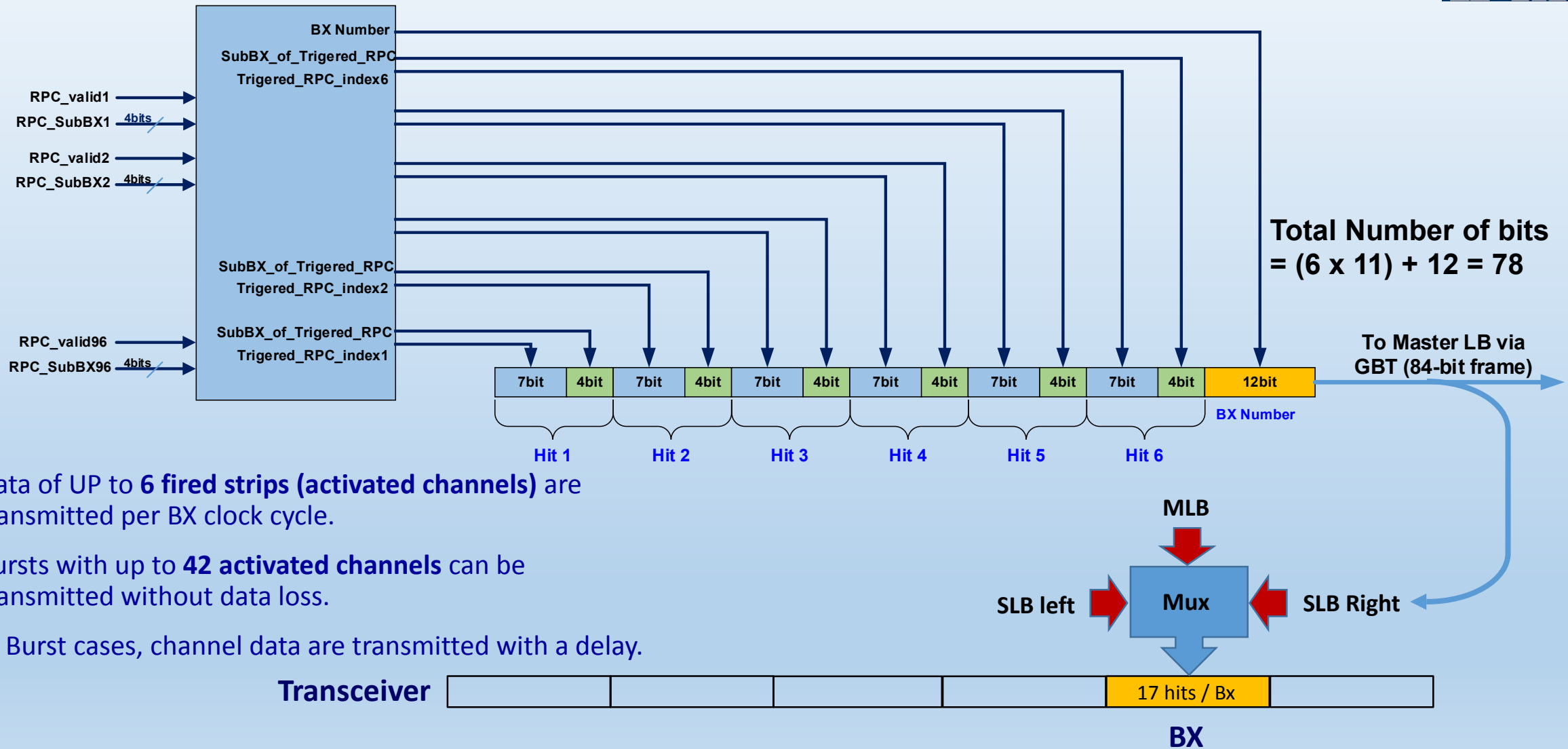
The first step of the RPC signal processing is the measurement of RPC signal arrival time and assignment of this data to the phase compensated LHC/CMS clock (40 MHz).



# Time-Stamping – TDC Transfer Function

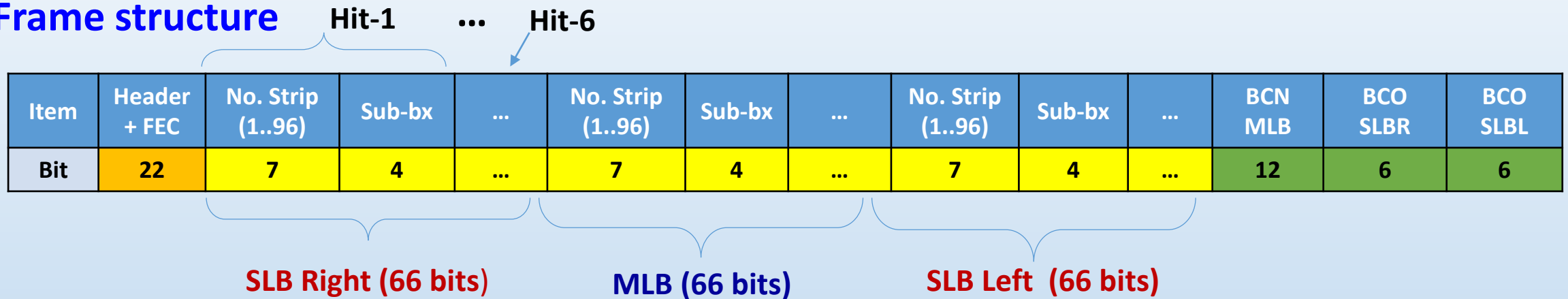


- ✓ TDC resolution is 1.56 ns. The gain error is zero but the offset error is not.
- ✓ TTC clocks and RPC hit signals have delays w.r.t the origin of the LHC clock. This cause a fixed offset error on the TDC transfer function.
- ✓ In Link Board, the TDC data is compensated with two parameters; 1) Macro steps: 1.56 ns, and 2) Micro steps: 48 ps. Figure left, Macro step offset error compensation, and Figure right, Macro + Micro steps offset error compensation.



- Data of UP to **6 fired strips (activated channels)** are transmitted per BX clock cycle.
- Bursts with up to **42 activated channels** can be transmitted without data loss.
- In Burst cases, channel data are transmitted with a delay.

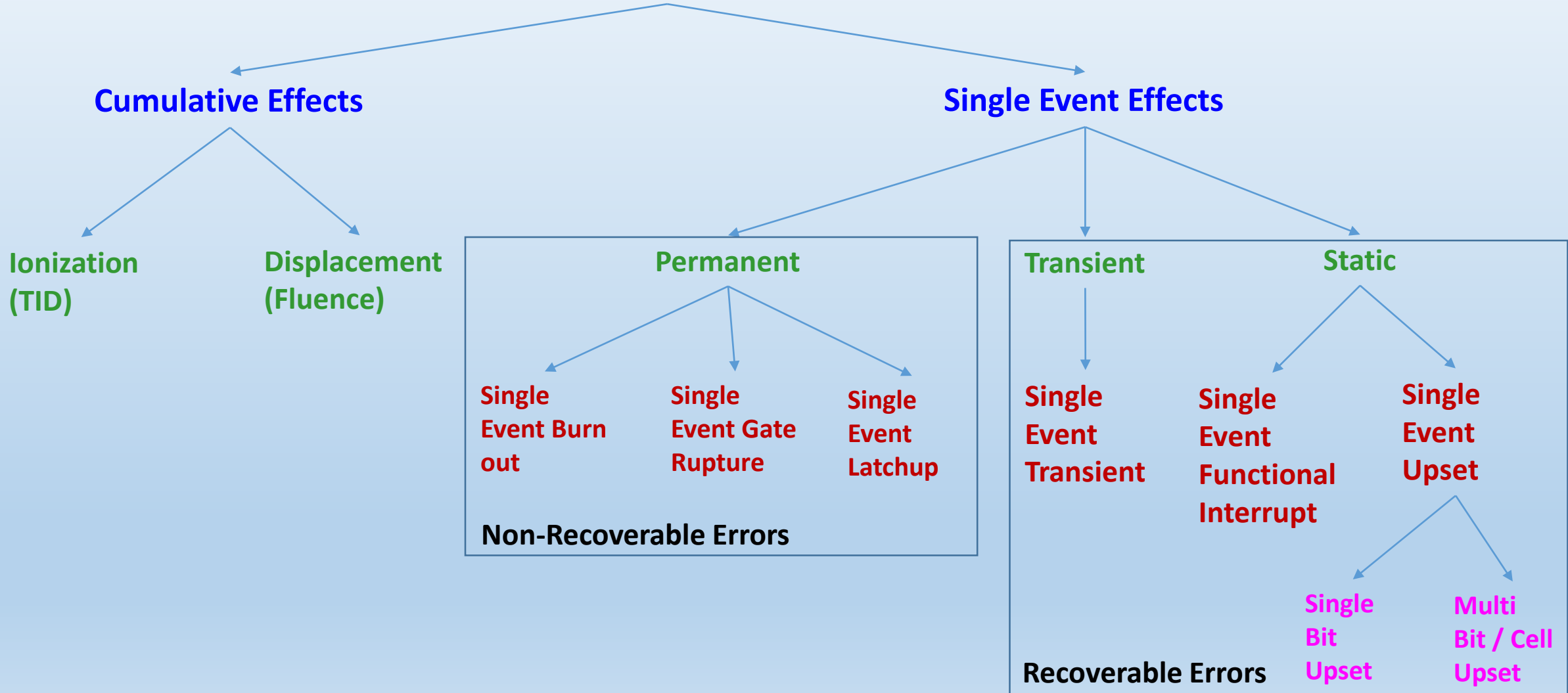
## • Frame structure



## • Frame Fields

- **Overhead electronics:** Header (2 bits) + FEC (20 bits)
- **Hit information:**
  - The number of fired strips could be between strip no. 1 to strip no. 96. Size of this field is 7 bits.
  - The Sub-BX or fractional part of the hit time of a fired strip. The size of this field is 4 bits.
- **Master LB Bunch Crossing:** Sets as a reference and keeps in the **BCN MLB**.
- **Bunch Crossing Offsets:** The Bunch crossing in the **Slave LB Right and Left** has an offset w.r.t the Master Link Board bunch crossing. These offsets keep in the **BCO SLBR/SLBL** fields.
- **Frame size:** 256 bits
- **Total Number of data bits:**  $(3 \times 66) + 12 + 6 + 6 = 222$  bits

## Radiation Effects



## Single Event Effects

Table 1. Non destructive SEE phenomena.

Upset - SEU <sup>1</sup>	corruption of the information stored in a memory element	Memories, latches in logic devices
Multiple Bit Upset - MBU	several memory elements corrupted by a single strike	Memories, latches in logic devices
Functional Interrupt -SEFI	loss of normal operation	Complex dev. with built-in state/control section
Transient - SET	impulse response of certain amplitude and duration	Analog and Mixed Signal circuits, Photonics
Disturb - SED	momentary corruption of the information stored in a bit	combinational logic, latches in logic devices
Hard Error - SHE	unalterable change of state in a memory element	Memories, latches in logic devices

Table 2. Destructive SEE phenomena.

Latchup - SEL	high-current conditions	CMOS, BiCMOS devices
Snapback - SESB	high-current conditions	N- MOSFET, SOI devices
Burnout - SEB	destructive burnout	BJT, N-channel Power MOSFET
Gate Rupture - SEGR	rupture of gate dielectric	Power MOSFETs
Dielectric Rupture - SEDR	rupture of dielectric	Non-volatile NMOS struct., FPGA, linear devices...

## Cumulative Effects

Table 3. Typical TiD degradation modes in devices.<sup>2</sup>

<i>device</i>	<i>Degradation mode</i>
MOS	Shifting of threshold voltage
BJT	Current gain degradation
Digital circuits	Increased leakage current (Iccop, Icc-sb), reduced retention time (DRAMs and SDRAMs)
Linear devices	Increased Offset voltage and bias current

Table 4. Typical DD degradation modes in circuits.

<i>device</i>	<i>Degradation mode</i>
CCD/APS	Reduced responsivity (Increase of dark current, RTS occurrence... <sup>o</sup> )
Bipolar Linear devices	Gain degradation
Solar cells	Reduced efficiency (output power, short circuit current)
Laser diode	Threshold current increase

Reference: R. Velazco et al. (eds.), *Radiation Effects on Embedded Systems*, 201–251. © 2007 Springer.

- Two main standards are widely used within the framework of **SEE testing**:
  - 1) **ESA/SCC 25100**: Single Event effects test methods and guidelines
  - 2) **JEDEC JESD57**: Test procedures for the measurement of Single-Event Effects in semiconductor devices from heavy ion irradiation
  
- The SCC standard applies to proton and heavy ion testing whereas the JEDEC standard only addresses heavy ion testing.

Requirements	ESA/SCC 25100	JEDEC JESD57
Scope	Single Event effects test method and guidelines	Test procedures for the measurement of Single-Event Effects in semiconductor devices from <b>heavy ion</b> irradiation
Radiation sources and characteristics	HI : range $\geq 30\mu\text{m}$ , $10^2 \geq \text{Flux} \geq 10^5 \text{ ions/cm}^2.\text{s}$ p+ : 20-300 MeV $10^5 \geq \text{Flux} \geq 10^8 \text{ ions/cm}^2.\text{s}$	range large compared to the depth of the collection region, $10^2 \geq \text{Flux} \geq 10^5 \text{ ions/cm}^2.\text{s}$ LET up to 120 MeV/mg.cm <sup>2</sup>
Dosimetry	Uniformity $\pm 10\%$ over the device area Flux $\pm 10\%$	Energy $\pm 10\%$ Uniformity $\pm 10\%$ over the device area Flux $\pm 10\%$
Testing requirements	Sample size $\geq 3$ (same dtc) 5 measurements at different effective LETs (HI) or Energies (p+, normal incidence) Max fluence of resp. $10^7$ and $10^{10}$ part./cm <sup>2</sup> .s for HI and p+ or a meaningful number of events	Measurements at onset threshold, 10%, 25%, 50% and 75-80% of the saturated $\sigma$ , Max fluence of $10^7 \text{ ions/cm}^2.\text{s}$ for “hard” devices, $10^6 \text{ ions/cm}^2.\text{s}$ or 100 events whichever comes first for “soft” devices Tilt angles limited to 60°

# Electronics validation Strategy

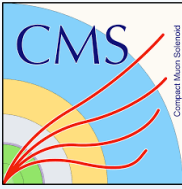
Step	Description	FPGA	ASIC	Goals
1	<b>Obtain</b> the SEU cross section of FPGA resources (Configuration Memory, BRAM, MGTs, FFs)	<ul style="list-style-type: none"> <li>✓ <math>\sigma_{\text{CRAM}}: 6.89 \times 10^{-15} \text{ (cm}^2\text{/bit)}</math></li> <li>✓ <math>\sigma_{\text{BRAM}}: 6.15 \times 10^{-15} \text{ (cm}^2\text{/bit)}</math></li> <li>✓ <math>\sigma_{\text{GTX}}: 7.27 \times 10^{-12} \text{ (errors/lane/cm}^2\text{/bit)}</math></li> </ul>	-	
2	<b>Estimate</b> of the Upset rate within the CMS radiation environment	✓	-	
3	<b>Cold-Test, Fault injection in Lab and</b>	✓ Firmware mitigation will be started after completion of the firmware integration	-	<ul style="list-style-type: none"> <li>❑ Evaluation of the rad-hard techniques</li> </ul>
4	<b>Hot-Test, (SEE)</b>	✓ Proton Beam / Heavy Ion cocktail	-	<ul style="list-style-type: none"> <li>❑ Evaluation of the rad-hard techniques adopted during the experiments must prevent build up of errors in different FPGA parts</li> <li>❑ Irradiations are done in vacuum and for most of the ions naked chips are needed.</li> </ul>
5	<b>Full Electronics Test (TID)</b>	<ul style="list-style-type: none"> <li>✓ 300 krad</li> <li>✓ <math>1.3 \times 10^{13} \text{ (proton/cm}^2\text{) without TIFR}</math></li> </ul>	<ul style="list-style-type: none"> <li>✓ Cobalt-60 or X-Ray</li> </ul>	<ul style="list-style-type: none"> <li>❑ Check the fault resilience of all electronics active devices such as FPGA, Digital and Analog ASICs, under X-Ray at 1 MeV Neutron Equivalent energy. <b>Exactly similar to Medical irradiation treatment.</b></li> </ul>

[1] Radiation testing campaign results for understanding the suitability of FPGAs in detector electronics, [10.1016/j.nima.2015.11.033](https://doi.org/10.1016/j.nima.2015.11.033), 2015.

# Main features of TID radiation types.

- Radioactive **Cs137** and **Co60** sources deliver gamma rays, two strong advantages:
  1. the very wide range of dose rates available
  2. the fact that the total dose is well controlled in the device thickness.
- As photons delivered by Co60 have a large energy, **1.17 and 1.33 MeV**, dose uniformity is ensured.
- This advantage can be lost if the irradiation facility is not correctly filtered and delivers a sizeable ratio of low energy scattered photons inducing dose enhancements. Consequently, it is necessary to take care to correctly assess accurate dosimetry and use adequate filtering methods.

Radiation type	Main advantages	Main drawbacks
Electrons (accelerator)	High dose rate available Representative of some orbits	Costly Not adequate for low dose rates
Protons (accelerator)	High dose rate available Representative of some orbits	DD contribution Costly
X rays (photons)	High dose rates available Low cost	Dose enhancement effect Not adequate for low dose rates
Cs <sup>137</sup> & Co <sup>60</sup> sources (gamma rays)	Very large dose rate range Dose uniformity	Heavy shielding necessary Non-dominant in orbit



# Goals of the SEE Experiment

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## ➤ A SEE experiment aims

- ✓ evaluating in real-time the device's response under consecutive exposures with several beam characteristics.

## ➤ The final objective

- ✓ is to obtain a good description of the device behavior and an accurate measurement of its radiation response ( $\sigma(E)$  or  $\sigma(LET)$  for each error mode) to enable the calculation of reliable in-flight SEE rates.

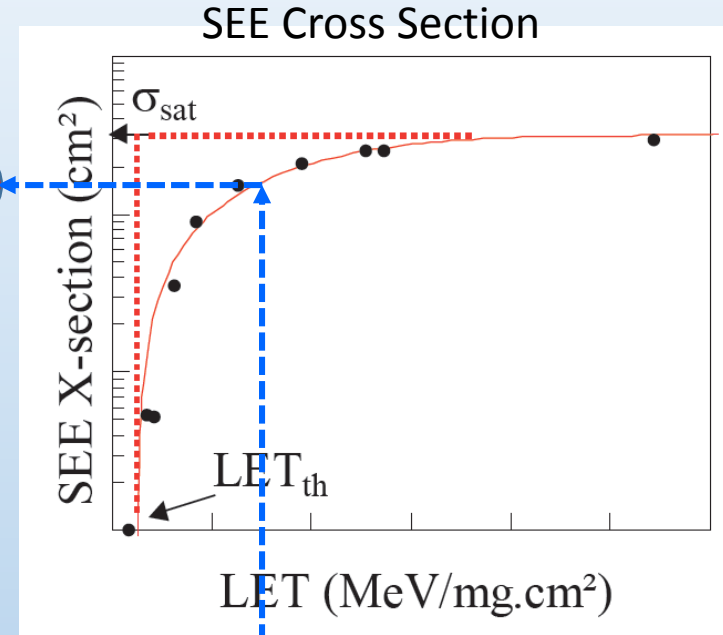
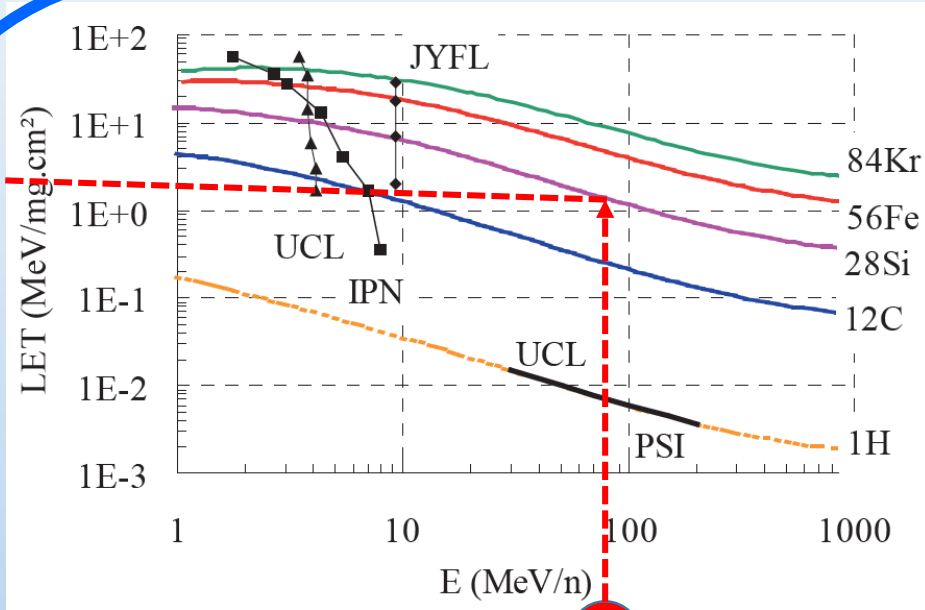
# How to measure the SEE

- $\sigma$  (LET) =  $\frac{\text{Number of SEE}}{\text{Fluence}}$  (units in  $\text{cm}^2$ )
- $\text{LET}(\theta) = \text{LET}(0^\circ) / \cos \theta$

- $\text{Number of SEUs} = \text{Fluence} \times \sigma$  (LET)

- $\sigma$  (LET) Correlated with LET
- LET Correlated with Particle or Ion beam Energy and Atomic mass of target material

# Linear Energy Transfer (LET)



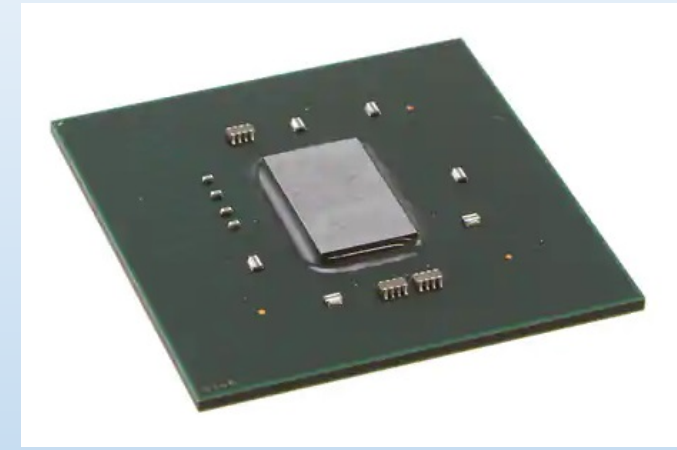
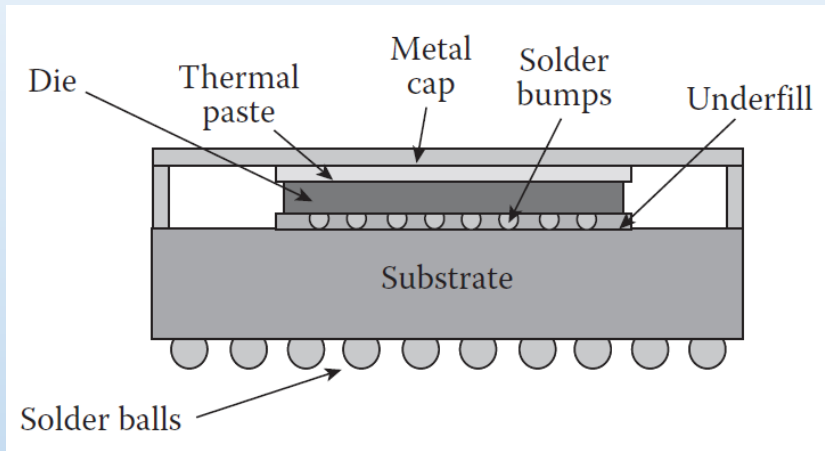
30 MeV proton beam  $\rightarrow$  LET  $1.469 \times 10^{-2}$  MeV cm<sup>2</sup> mg<sup>-1</sup>

$$t_{HL-LHC} = \frac{3000 \times 10^{39} \text{ cm}^{-2}}{1.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}} = 2.0 \times 10^8 \text{ s}$$

$$\sigma(\text{LET}) = \frac{\text{Number of Events}}{\text{Fluence}} \quad (\text{units in cm}^2)$$

$$\text{LET}(\theta) = \text{LET}(0^\circ) / \cos \theta$$

# Kintex7 Flip-chip Package



➤ Schematics of a flip-chip metallic package

➤ Link and Control Board Kintex-7 FPGA Flip-chip metallic Package

➤ Kintex-7 K160T Die after removing metal cap

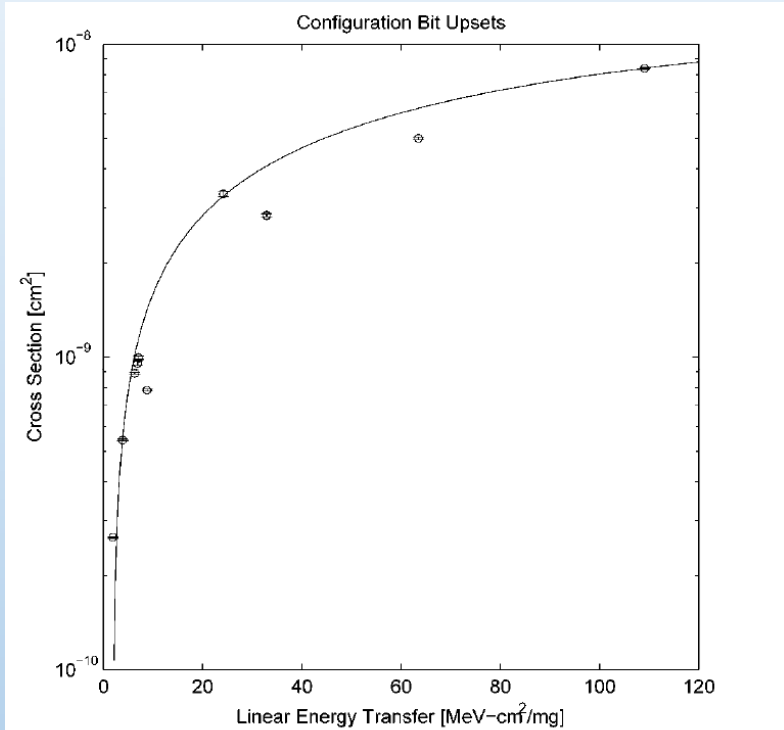


Fig. 1. Weibull curve for configuration memory cell upsets.  $L_{th}=1.9$  [MeV-cm<sup>2</sup>/mg],  $\sigma_{sat}=1.43e-8$  [cm<sup>2</sup>/bit],  $W=125.3$  [MeV-cm<sup>2</sup>/mg],  $S=0.78$ .

**Mitigation Technique:**  
Scrubbing

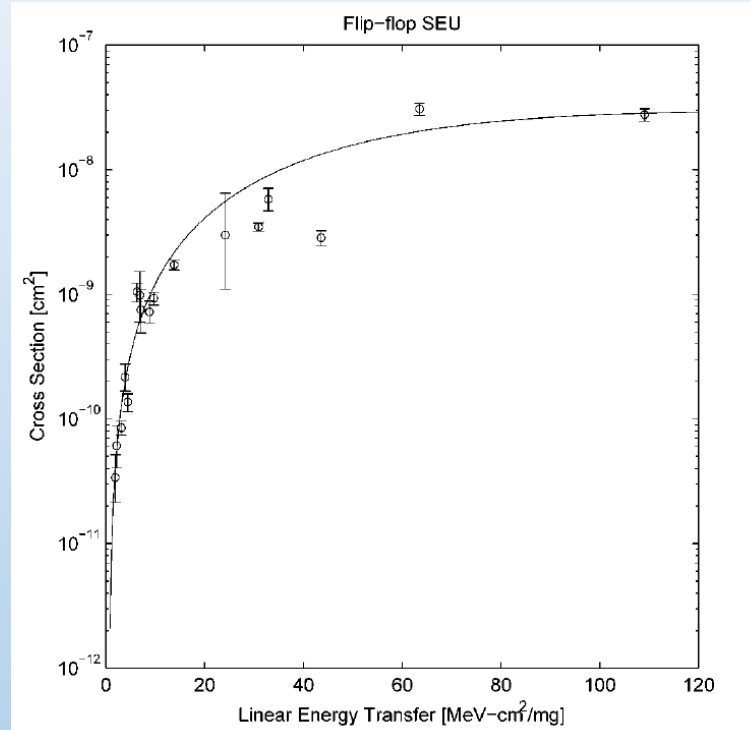


Fig. 3. Flip-flop memory cell SEU event Weibull curve.  $L_{th}=0.6$  [MeV-cm<sup>2</sup>/mg],  $\sigma_{sat}=3.0e-8$  [cm<sup>2</sup>/bit],  $W=58.4$  [MeV-cm<sup>2</sup>/mg],  $S=1.74$ .

**Mitigation Technique:**  
TMR

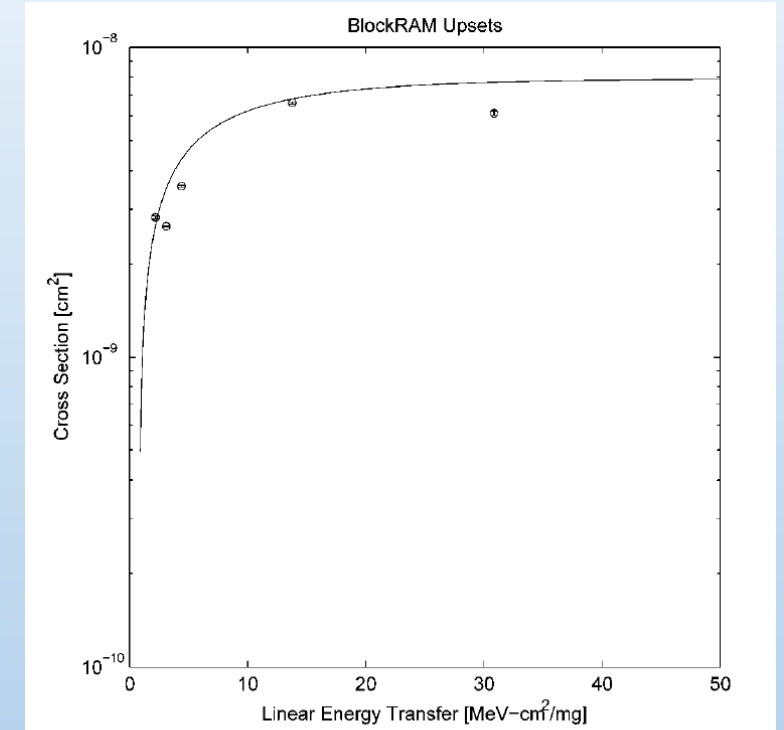


Fig. 5. BlockRAM SEU Weibull curve.  $L_{th}=0.8$  [MeV-cm<sup>2</sup>/mg],  $\sigma_{sat}=7.94e-9$  [cm<sup>2</sup>/bit],  $W=5.0$  [MeV-cm<sup>2</sup>/mg],  $S=0.7$ .

**Mitigation Technique:**  
ECC

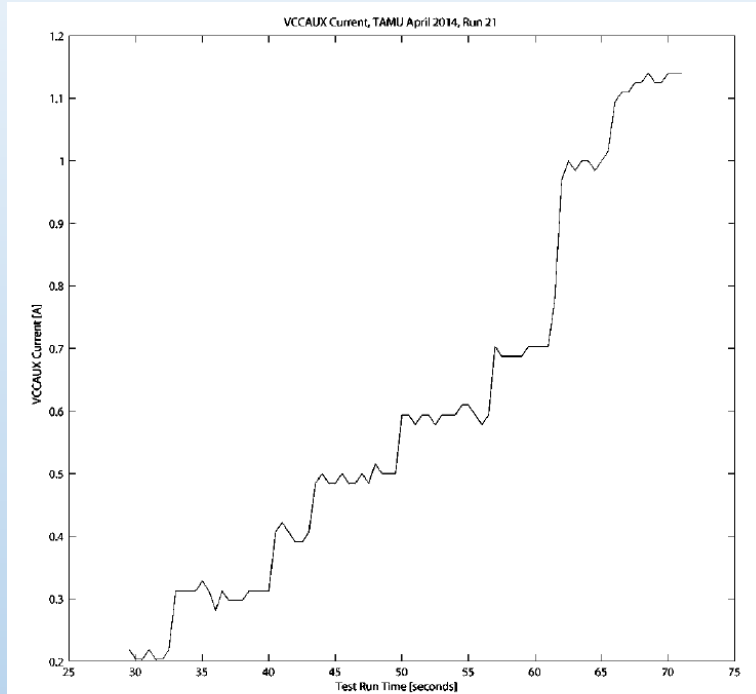


Fig. 6. Current strip chart taken during a SEL test run at TAMU, April 2014. Seven or eight SEL current-anomaly steps are clearly visible. Nominal current for this rail is  $210 \pm 16$  [mA].

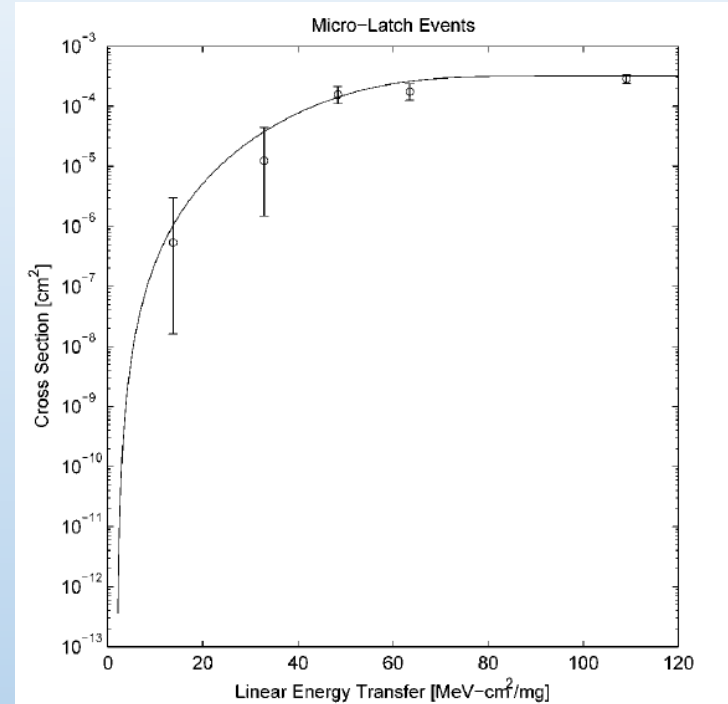


Fig. 7. Weibull curve for current-step events observed during SEL testing.  $L_{th}=1.9$  [MeV-cm<sup>2</sup>/mg],  $\sigma_{sat}=3.16e-4$  [cm<sup>2</sup>/bit],  $W=53.4$  [MeV-cm<sup>2</sup>/mg],  $S=3.8$ .

**Mitigation Technique:**  
**RESET, Flash-reloading,**  
**Power recycling**



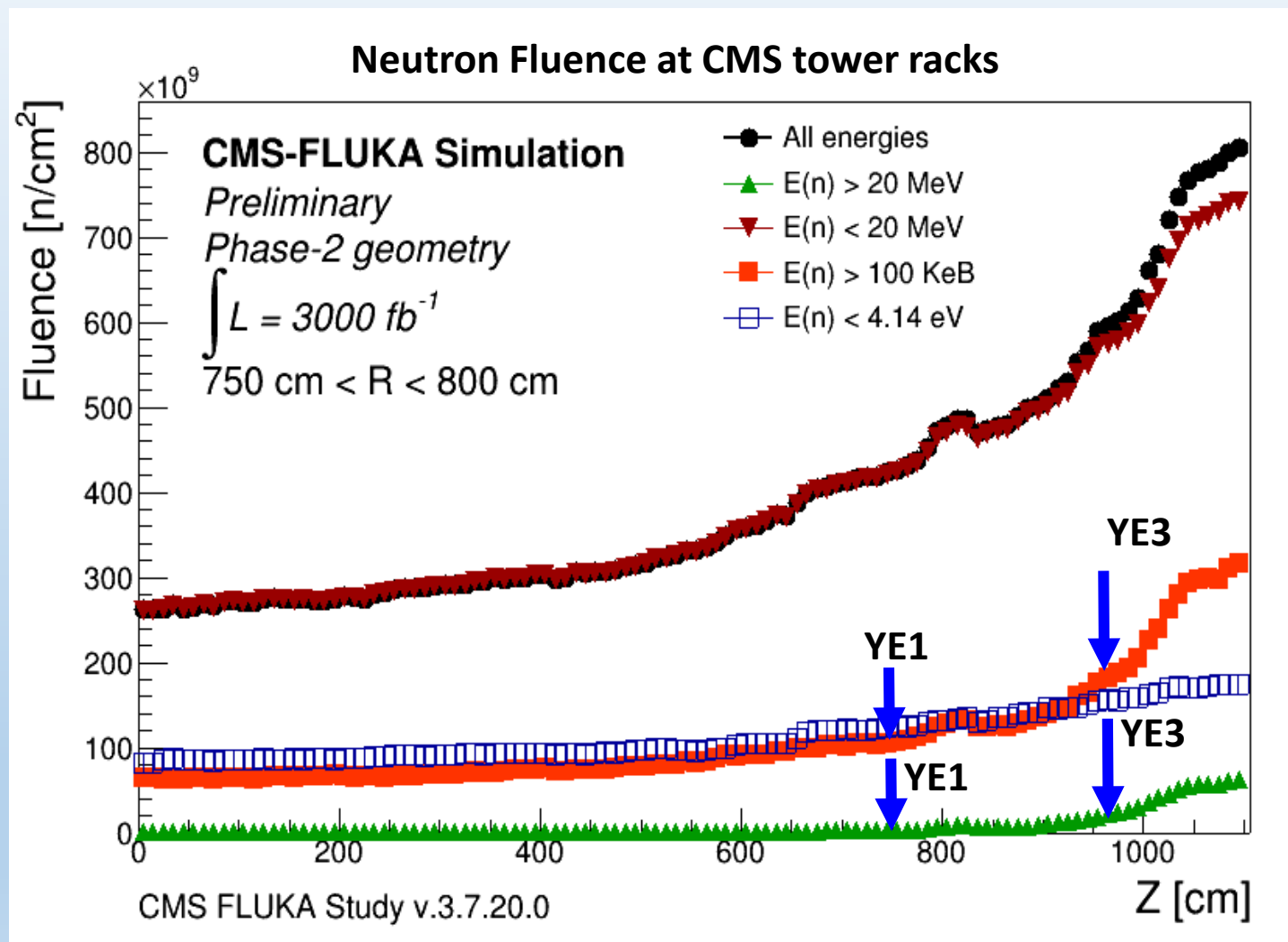
# Test facilities and domain of application



- **SEE characterization** of devices requires real-time testing under exposure (functional testing mainly), and the use of particle accelerators.
- **TID assessment** implies the full parametrical characterization at different step of dose levels received (sequence of irradiation/testing phases). Mostly, 60Co sources are used for irradiating.
- **DD testing** is quite similar to TID characterization as parametrical measurements and functional checking occurs at different received fluence levels (leading to an equivalent displacement damage dose - DDD6). However, DD testing requires the use of particle accelerators.

Standards	Effect	Parameters of concern
ESA-SCC 22900.4	<b>TID</b>	Total dose, dose rate
MIL-STD 883E Method 1019.6	<b>TID</b>	Total dose, dose rate
ESA-SCC 25100.1	<b>SEE</b>	LET/range (heavy ions), Energy (protons)
JESD57	<b>SEE</b>	LET/range (heavy ions)
ESA-SCC 22900.4	<b>DD</b>	Energy

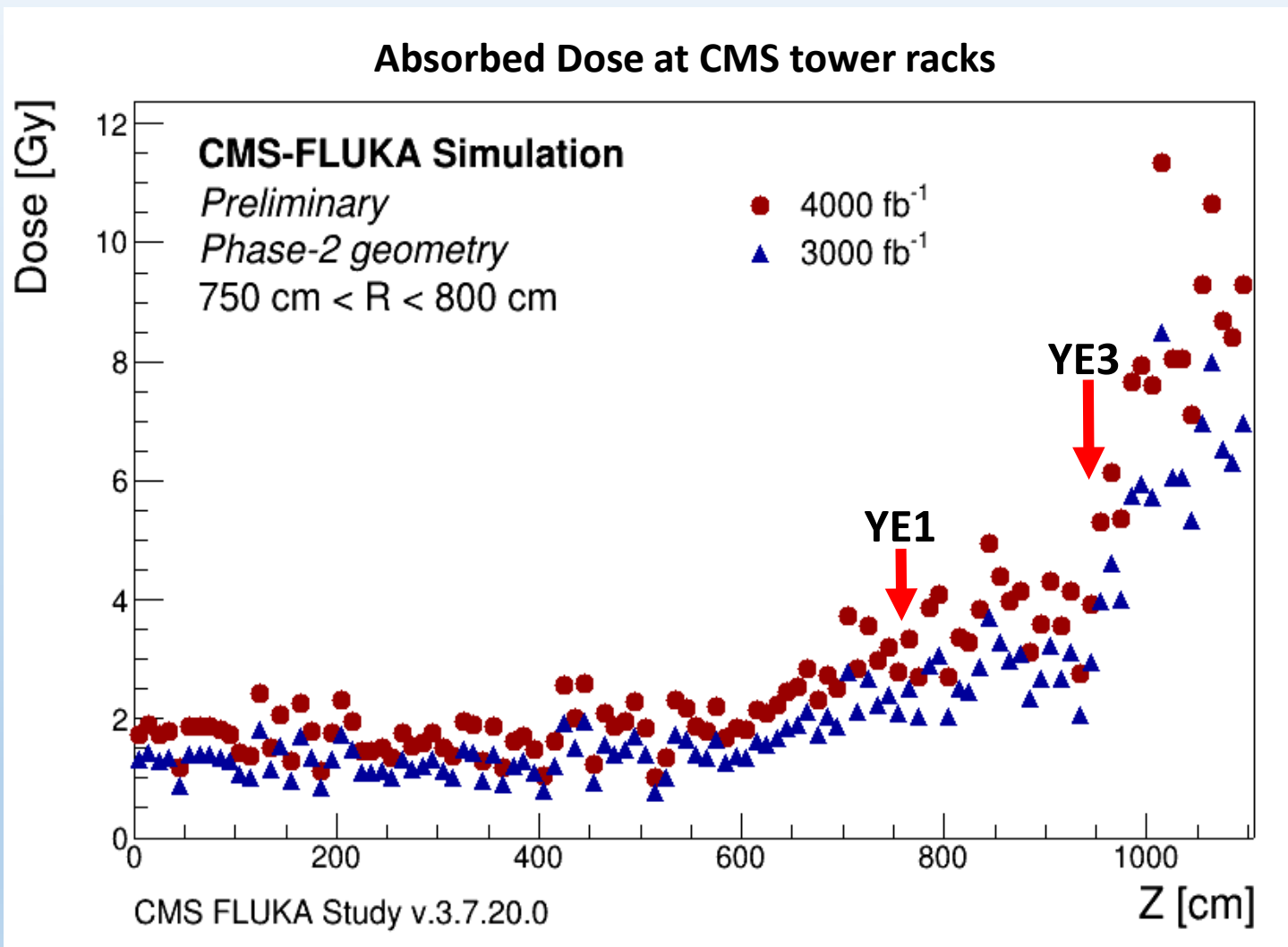
- Link System will install on the CMS Tower racks.
- Among all racks, the ones in front of the YE3 and YE1 are at higher exposure.



**Epithermal Neutrons**  
**Fluence at YE3 tower racks**  
 $< 1.6 \times 10^{11} \text{ n}/\text{cm}^2$

**20 MeV neutron Fluence**  
**at YE3 tower racks**  
 $< 2 \times 10^{10} \text{ n}/\text{cm}^2$

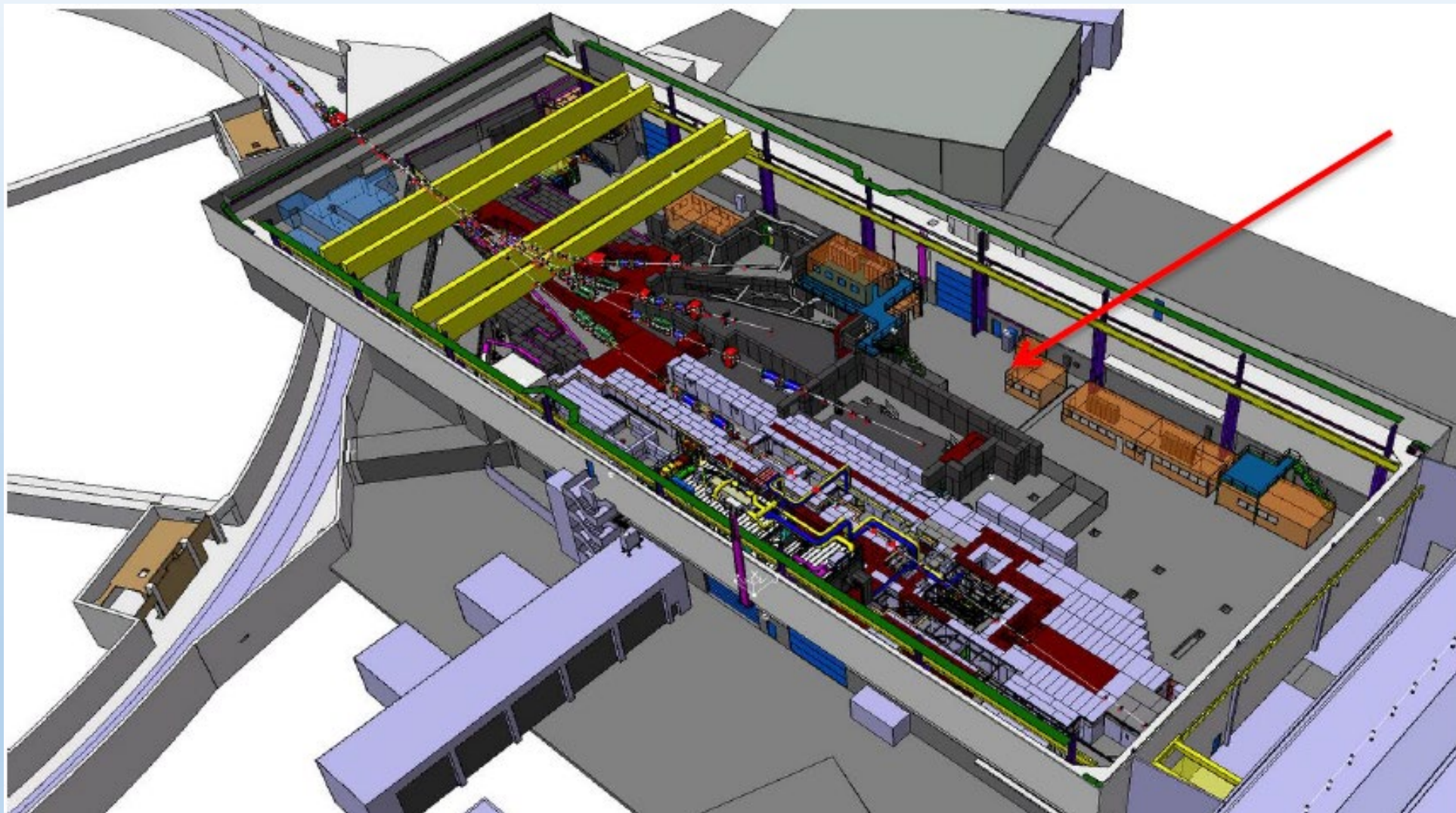
- Link System will install on the CMS Tower racks.
- Among all racks, the ones in front of the YE3 and YE1 are at higher exposure.



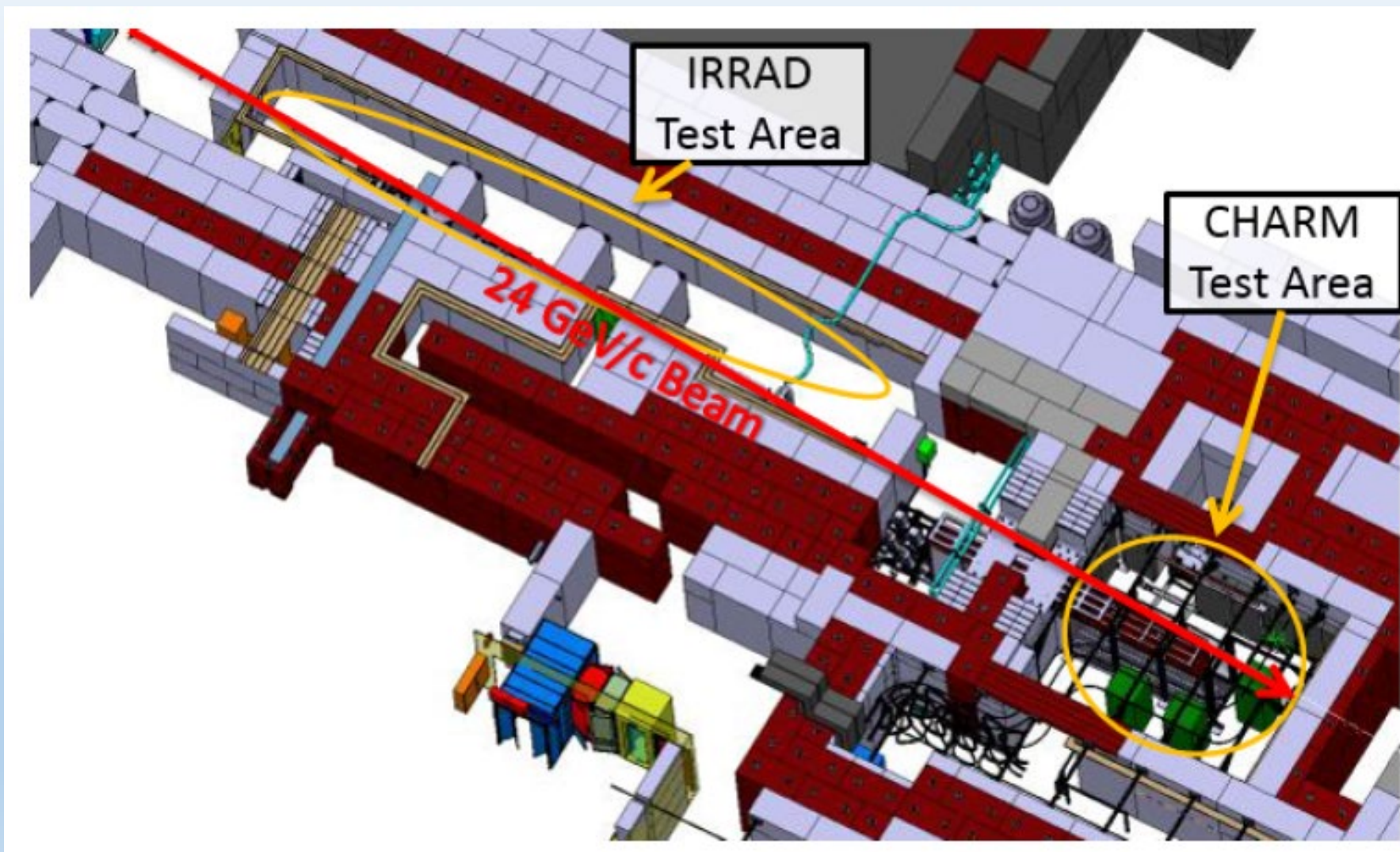
Integrated Dose  
at YE3 tower racks  
< 6 Gy



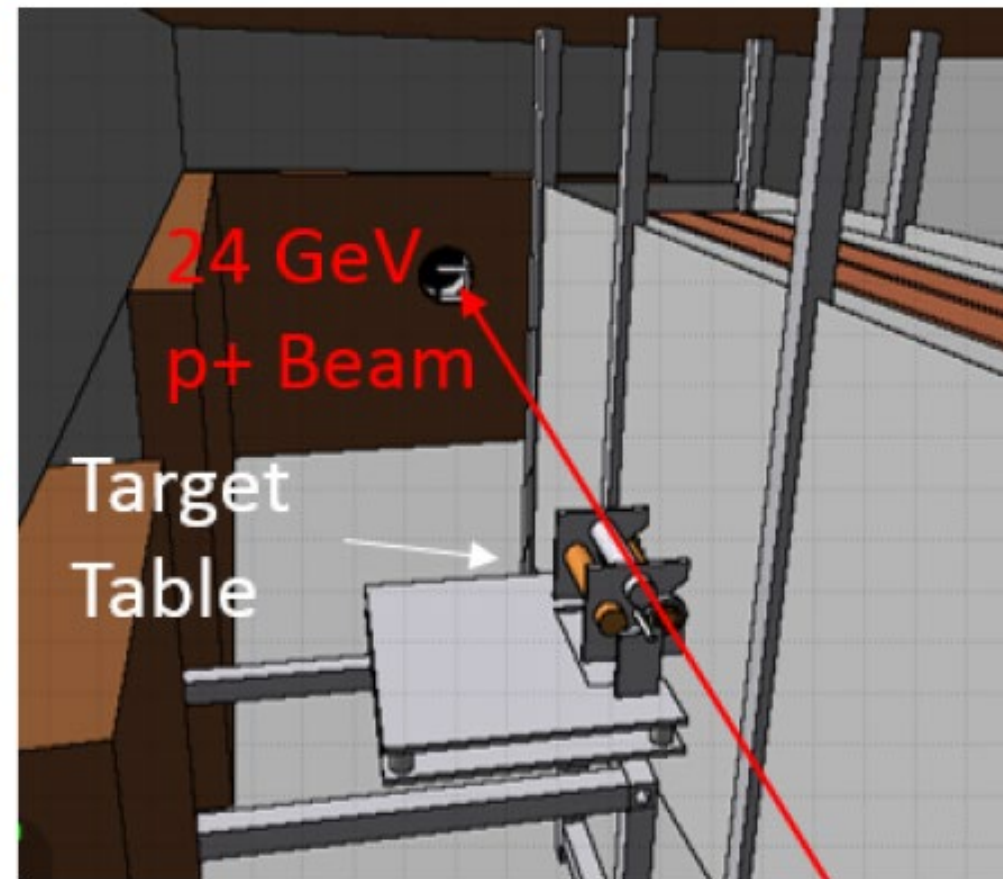
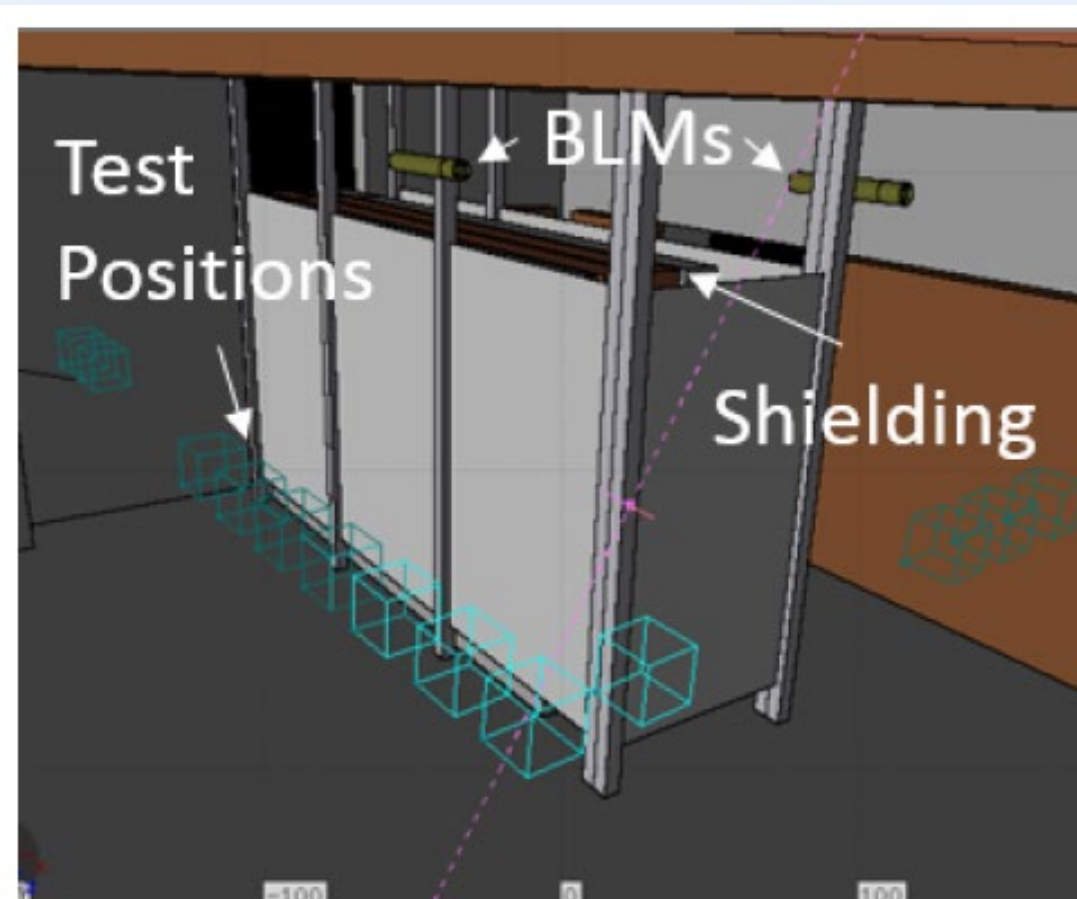
# The CHARM Irradiation Facility Layout



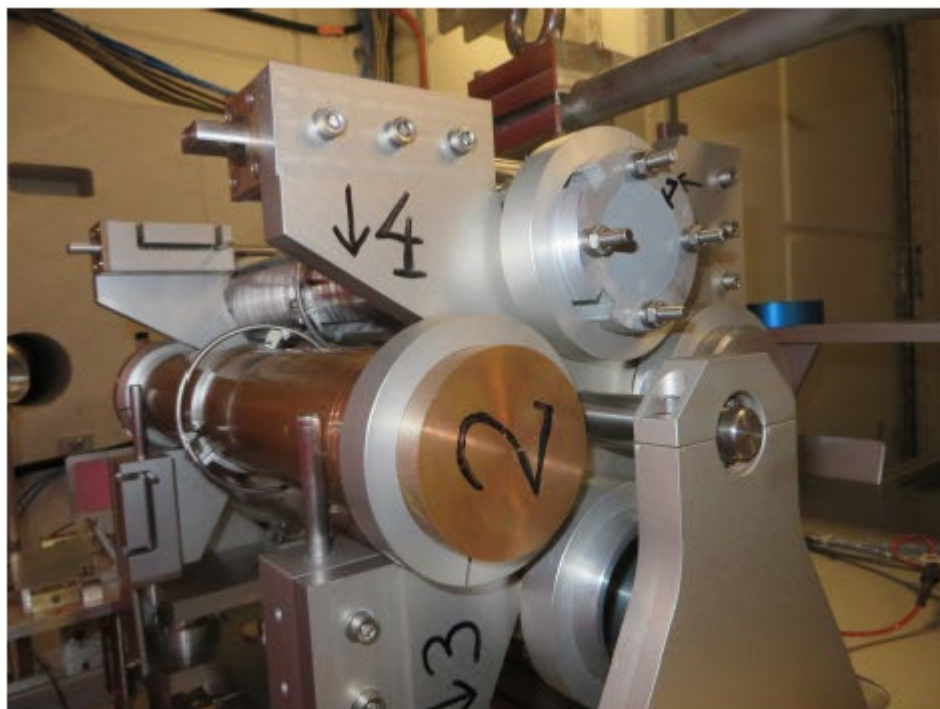
# The CHARM Irradiation Facility Layout



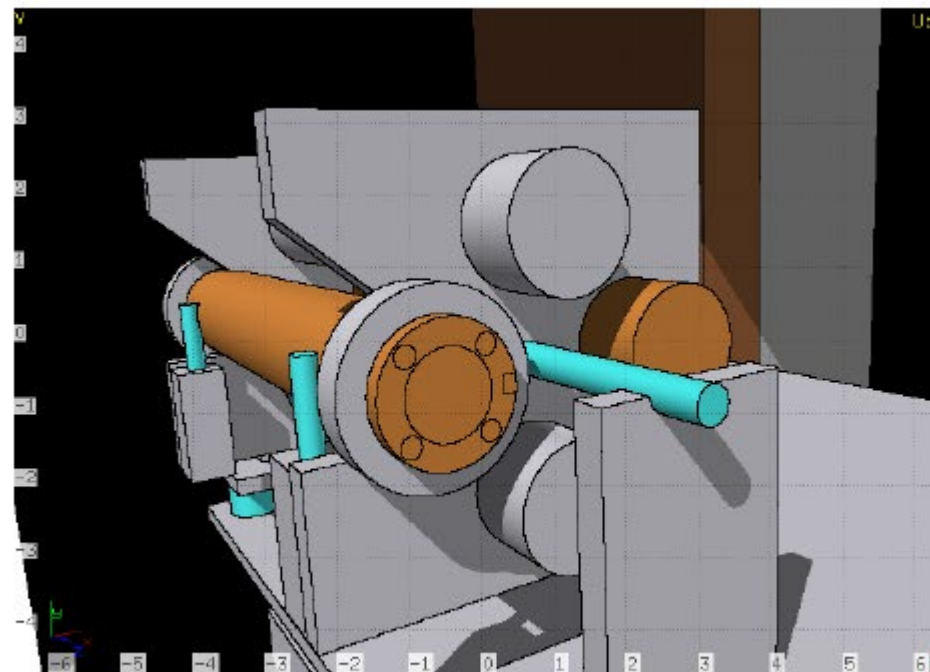
# The CHARM Irradiation Facility Layout



# The CHARM Irradiation Facility Layout

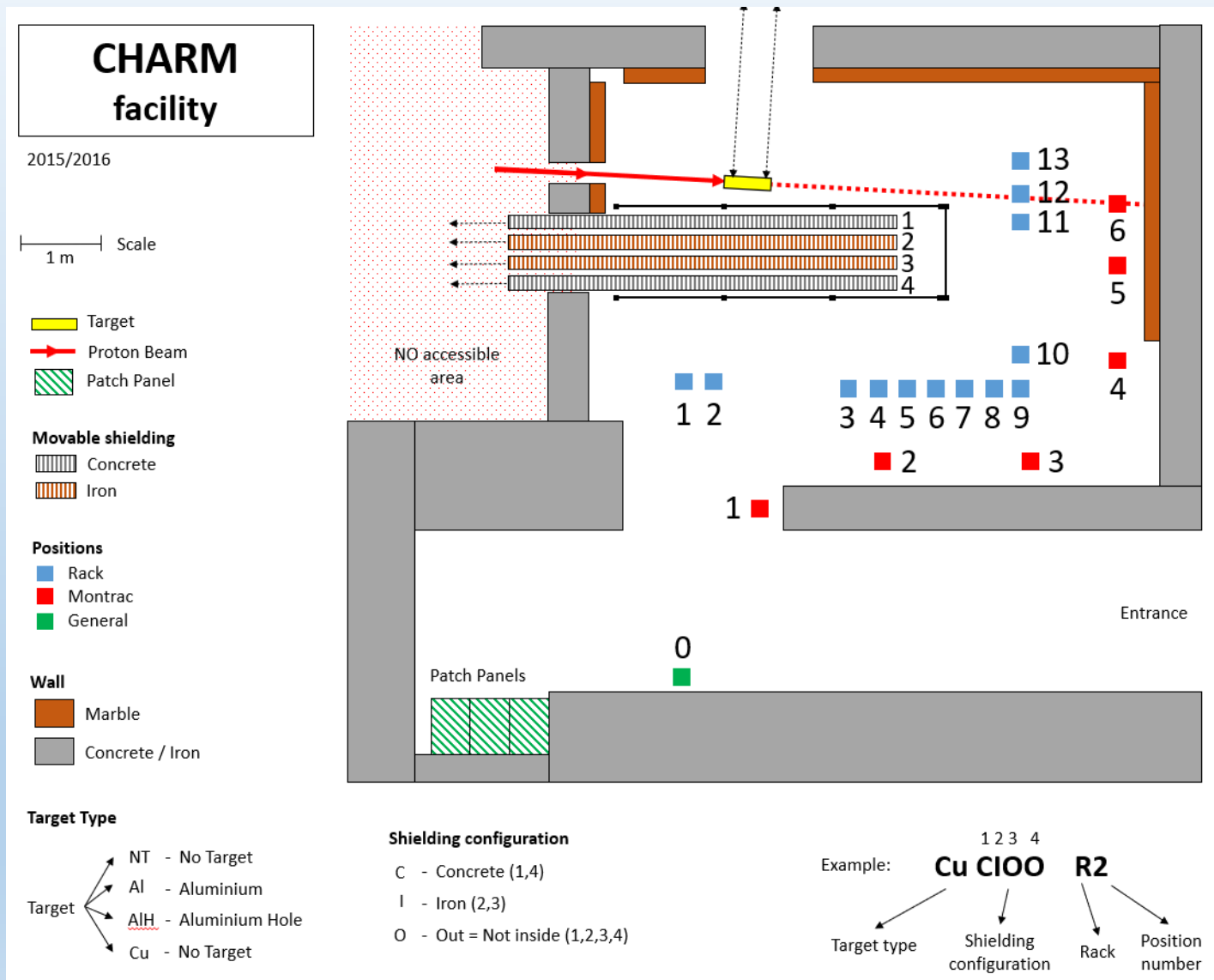


(a) A photo of the target table.



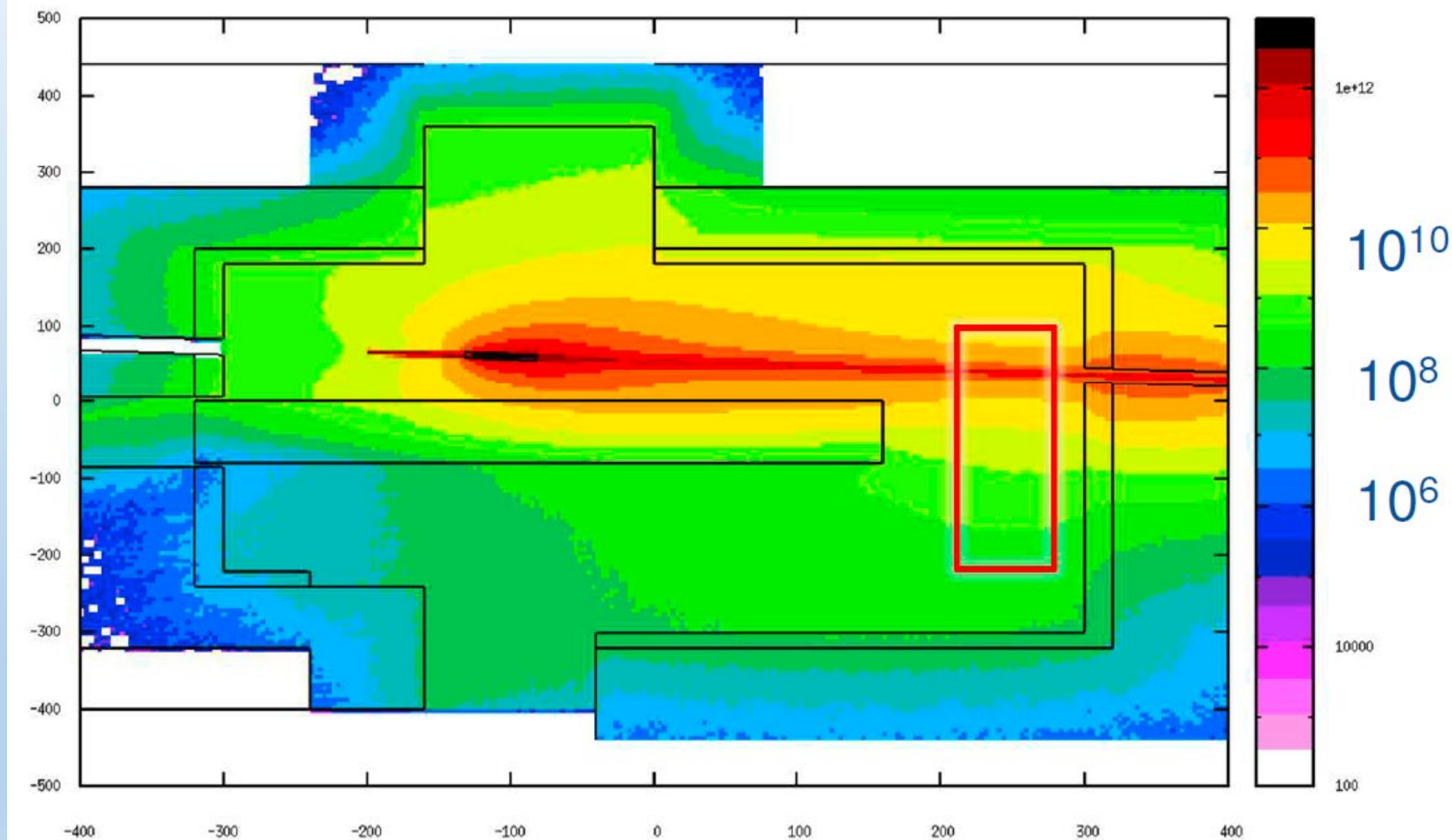
(b) A screen-shot from the FLUKA geometry

# The CHARM Irradiation Area II



# The CHARM Radiation Environment

HEH flux ( $\text{cm}^{-2}\text{h}^{-1}$ )



In the downstream locations (10-13) HEH fluxes of  $\sim 10^{10} \text{ cm}^{-2}\text{h}^{-1}$  (roughly one year in the LHC tunnel) can be reached in one hour

# The CHARM Radiation Environment

of the mixed-field environment, is that of a quasi-uniform spill lasting roughly 350 ms, which is repeated every 10 seconds. Although this would indeed be a pulsed beam for

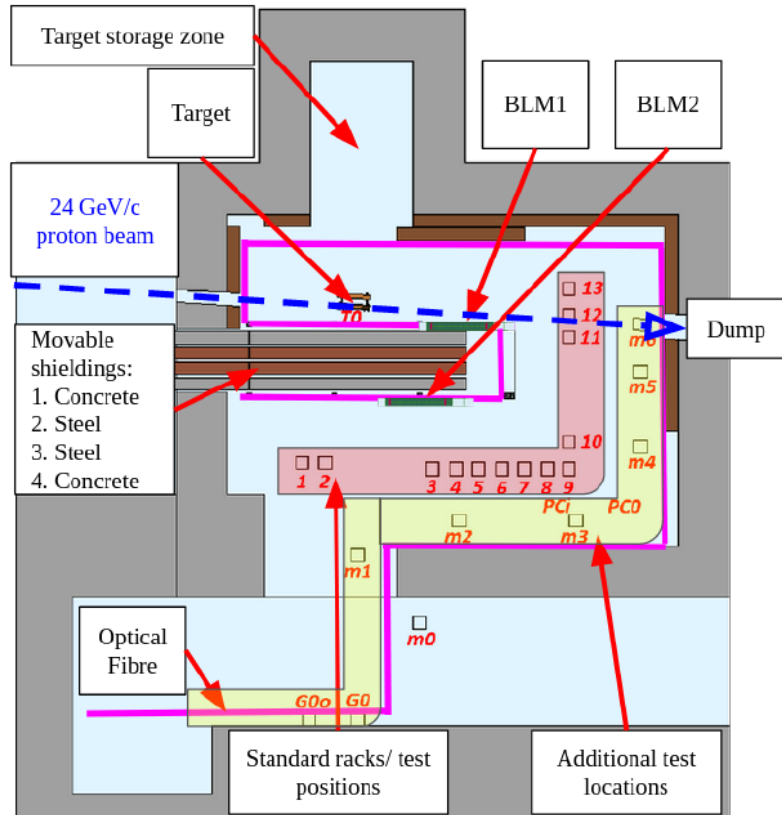
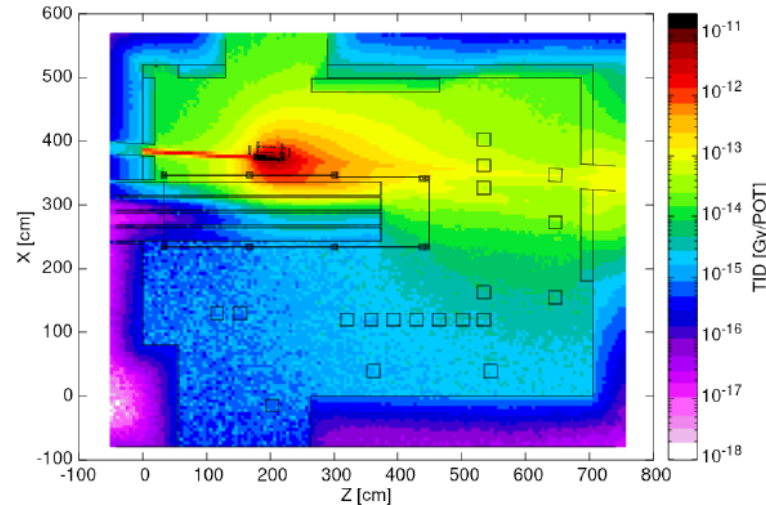
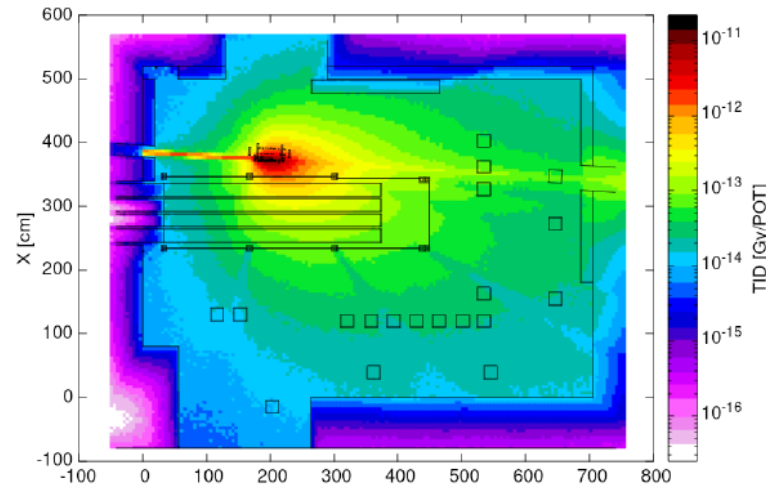


Fig. 1: Top view of FLUKA geometry of the CHARM test area. Two BLMs are installed at 1 m above beam height, one next to the target and one behind the movable shieldings. There



The simulated 2D TID distribution at beam height is shown for two configurations: **CuO000 (top)** and **CuCSSC (bottom)**.

[Paper Link](#)

# Wall grid (Position G0)



# CHARM Preparation Area

☐ September 2022: Dry-Run test for one week

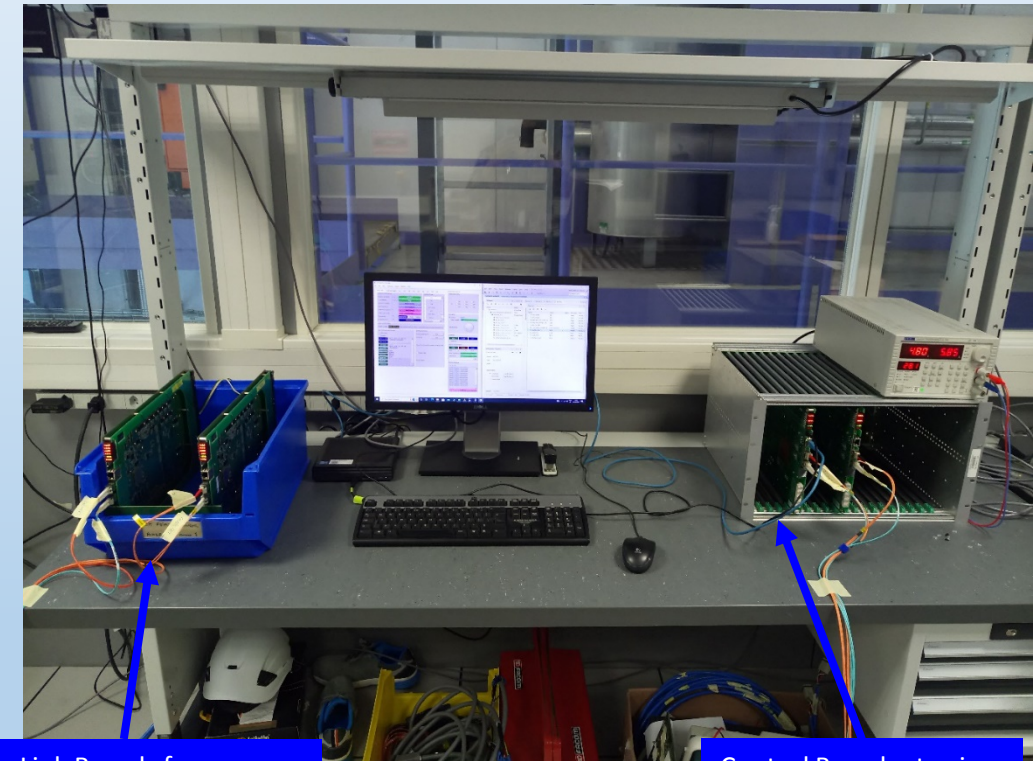
A copy of Patch Panels in the Control Room

A copy of Patch Panels in the Irradiation Area



Fibers

LV Cables (28 meter)



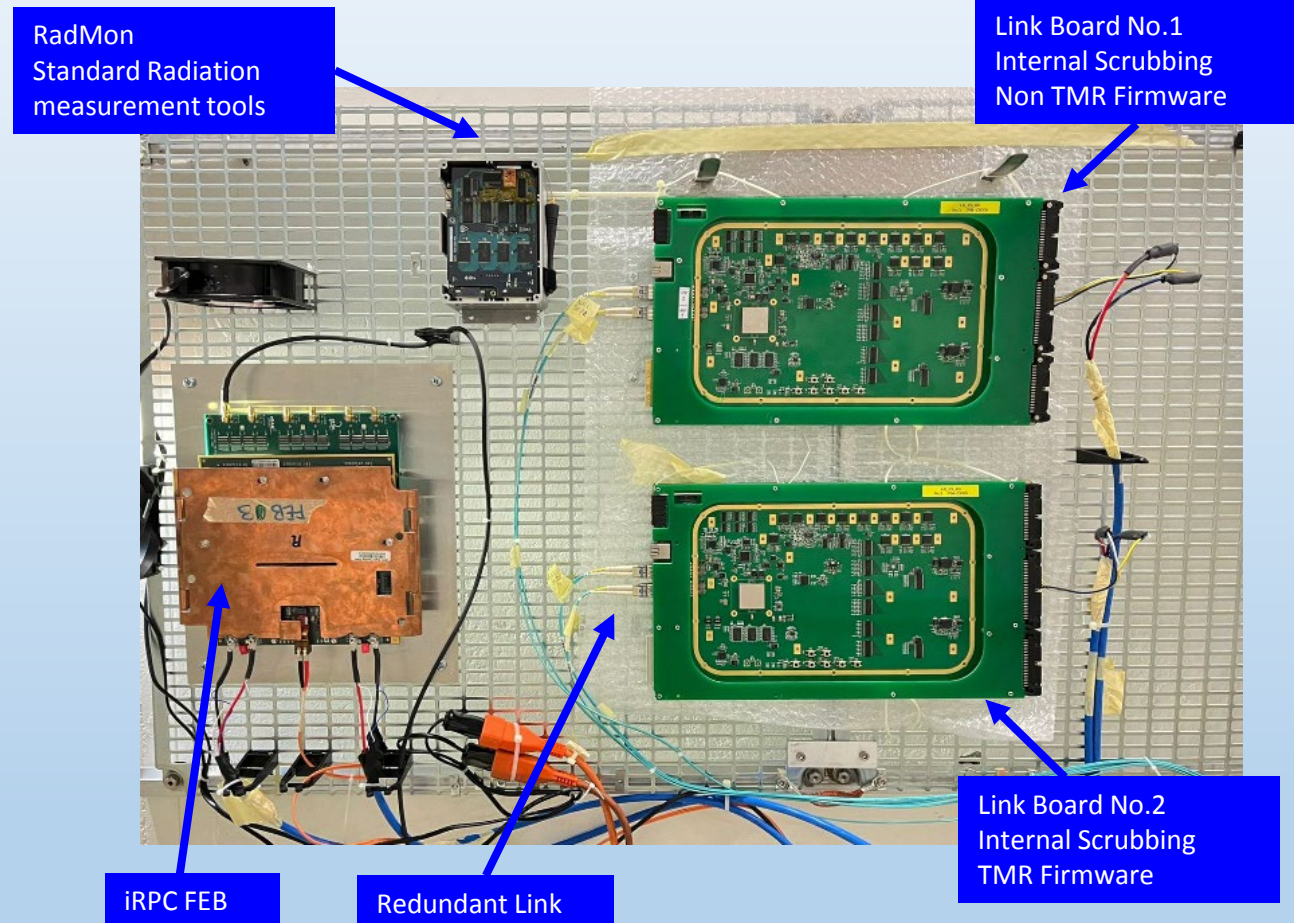
Link Boards for Irradiation Test

Control Boards stay in control room to read data

# Irradiation Test Setup in CHARM

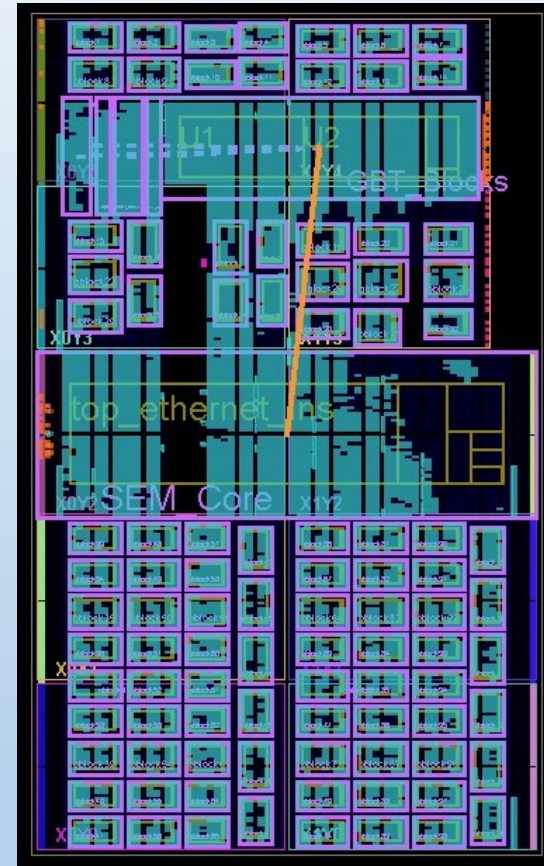
## Oct. 12-Nov. 1st: Irradiation Test for 3 weeks

- ✓ CHARM location G0
  - ✓ TID: 3.45 Gy/Day
  - ✓ Thermal neutron flux:  $2.7 \times 10^5$  ( $\text{cm}^{-2} \text{s}^{-1}$ )
  - ✓ High energy hadron flux:  $1.4 \times 10^5$  ( $\text{cm}^{-2} \text{s}^{-1}$ )
- ✓ Target for 10 years HL-LHC
  - ✓ 4000  $\text{fb}^{-1}$
  - ✓ Location of Installation on CMS tower racks
  - ✓ TID < 6 Gy
  - ✓ Total High and Low energy neutron flux <  $1.8 \times 10^3$  ( $\text{cm}^{-2} \text{s}^{-1}$ )
- ✓ Hardware Test Setup on the Charm
  - ✓ Two Link Boards is chosen for this test.
  - ✓ Link Board and Control Board is designed based on the same electronics devices and their circuits are very similar above 90%. For this reason, we decided to test only Link Boards.
  - ✓ Each board has a redundant optical Links and an Ethernet interface (added in week 3<sup>rd</sup> of the test)
  - ✓ In the Link System, Loss of connection is consider as a failure

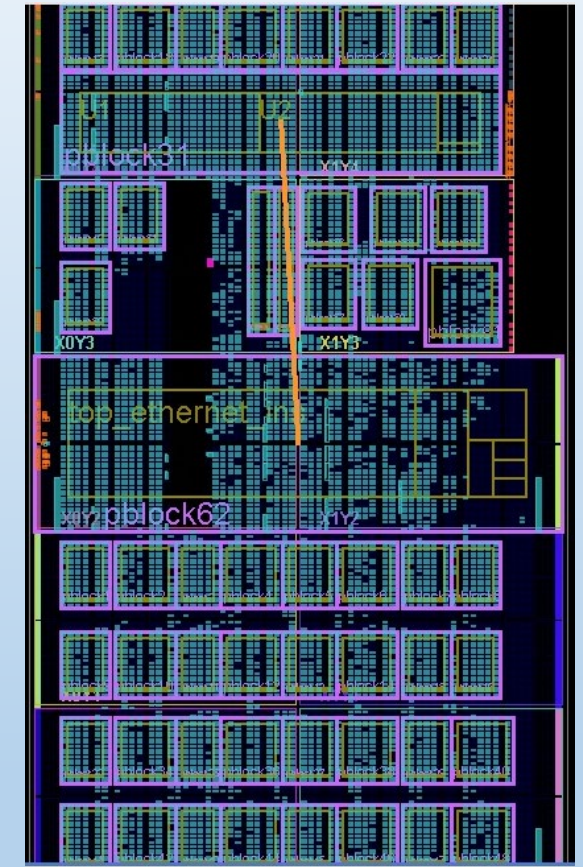


- ✓ CAEN power module, set a limit on the current to see the over-current and record the latch-up

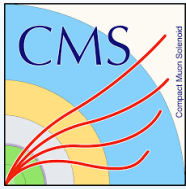
- Link Board firmware covers almost all logics and primitives expected to be used for HL-LHC.
- We have evaluated two mitigation techniques on the Link Board FPGAs (Kintex-7 XC7K160T):
  - Non-TMR + Internal Scrubbing (SEM)
  - TMR + Internal Scrubbing (SEM)
- In both firmware, a test logic block has been replicated over the entire FPGA to increase the chance of the SEUs and precisely evaluate the mitigation methods.
- Ninety-eight test blocks are implemented on the non-TMR firmware, and 37 TMRRed test logic blocks are replicated on the TMR firmware.
- Additionally, both firmware comprises two modified GBT-FPGA lanes, automatic link loss detection, and swapping, an Ethernet interface, Clock recovery and Jitter cleaner, and an SEM controller.



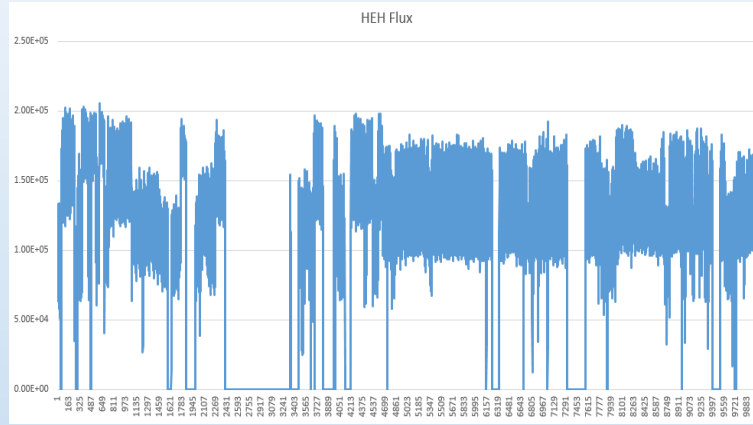
Kintex-7, TMR +  
Internal Scrubbing



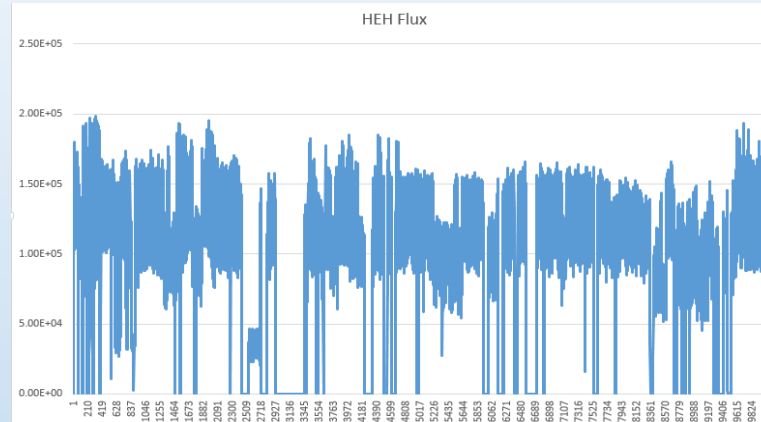
Kintex-7, non-TMR +  
Internal Scrubbing



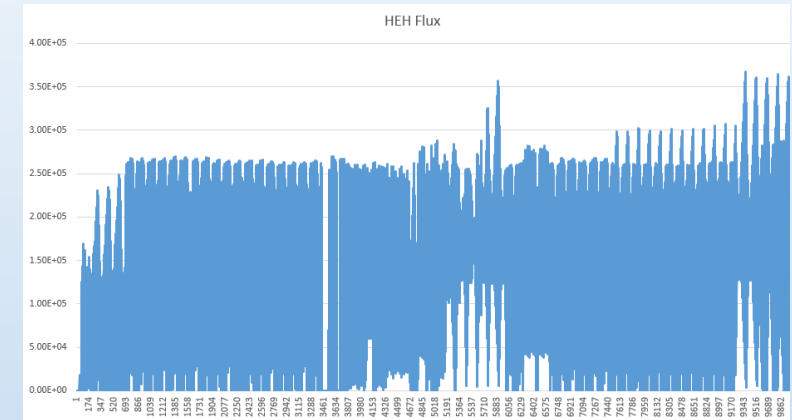
# HEH and ThN Flux at G0



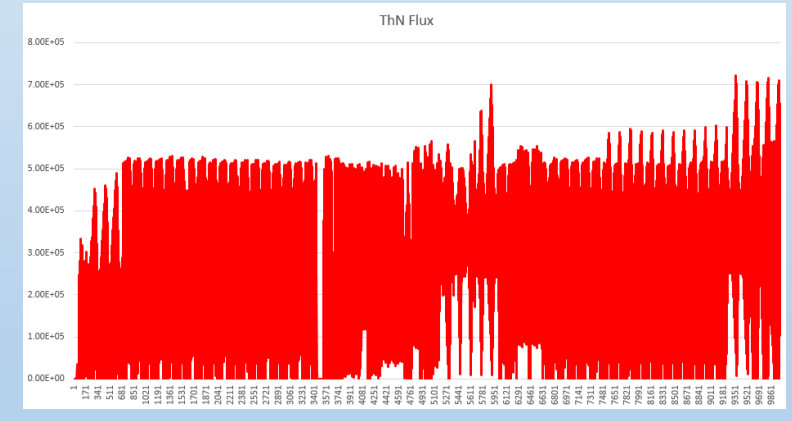
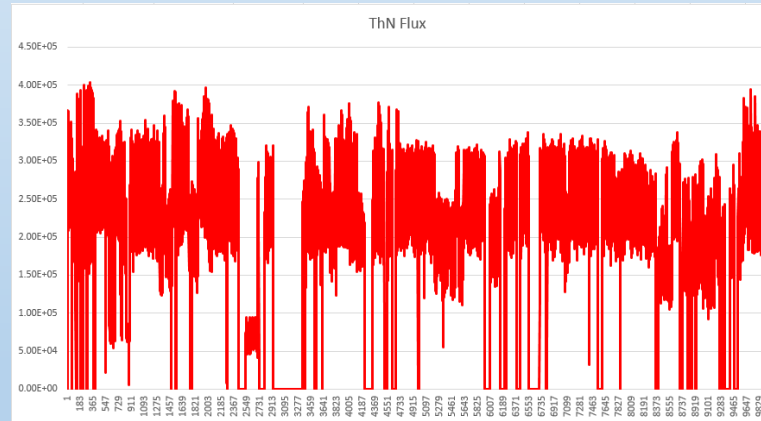
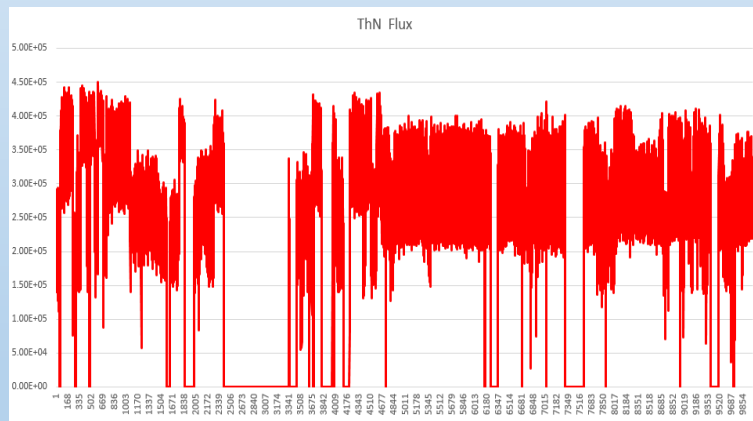
**RUN1**

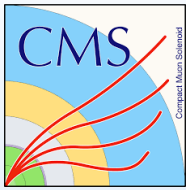


**RUN2**

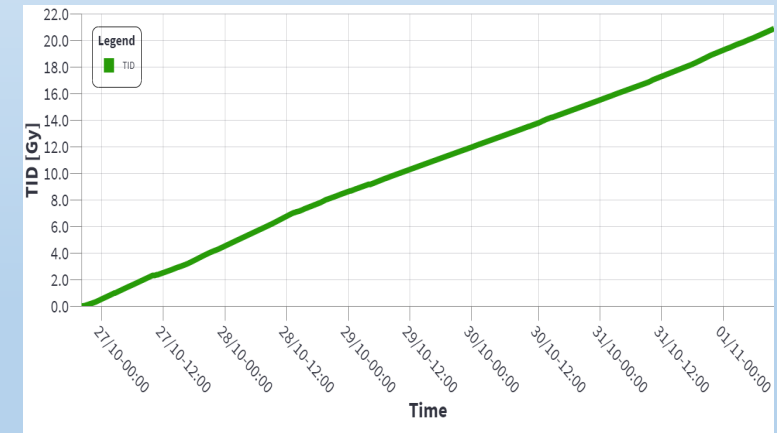
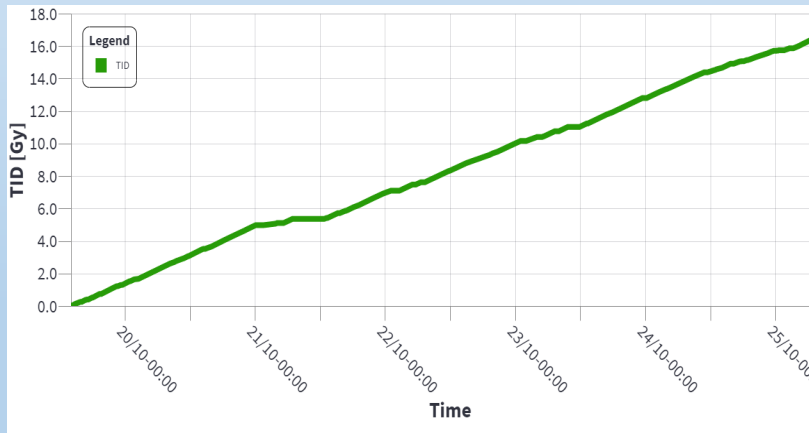
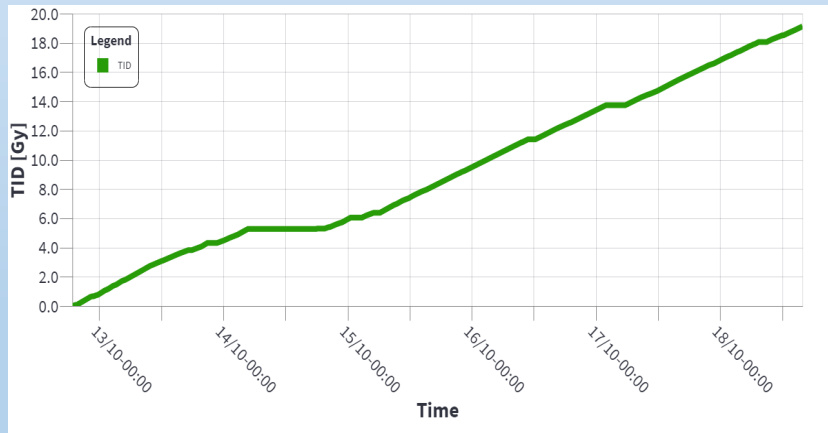
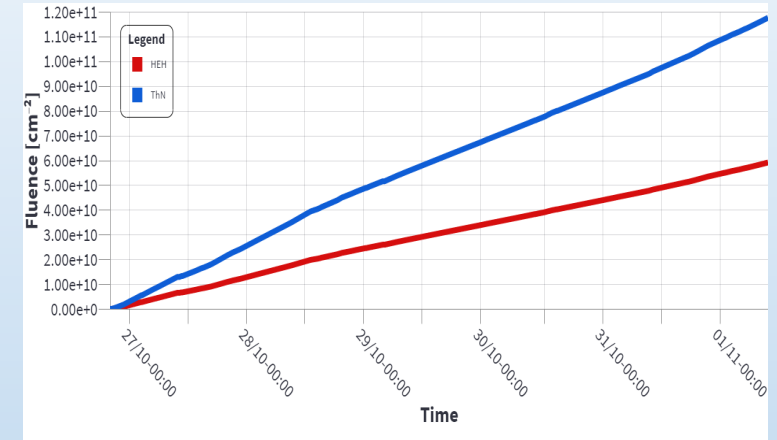
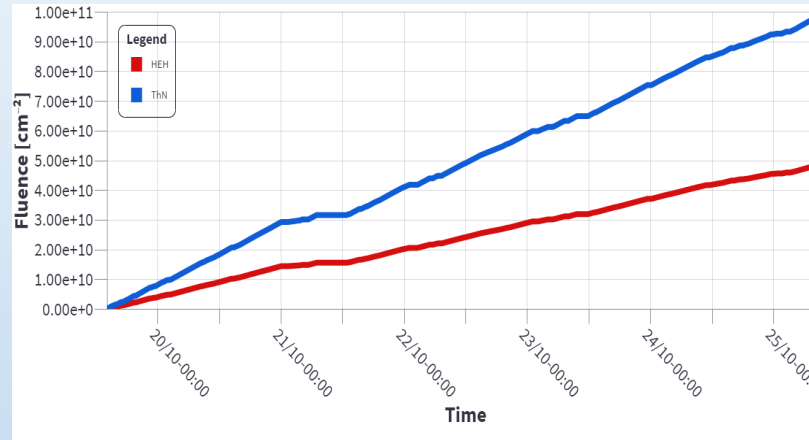
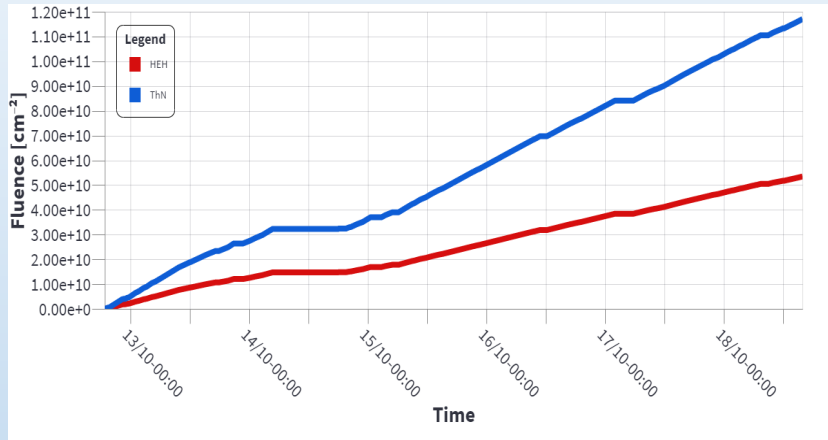


**RUN3**





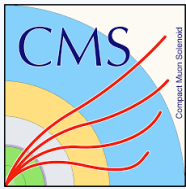
# HEH and ThN Fluence/TID at G0



**RUN1**

**RUN2**

**RUN3**



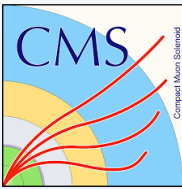
# Irradiation Test – Results

## ☐ Oct. 12-Nov. 1<sup>st</sup> 2022: Irradiation Test Results

- ✓ Electronics running for over three weeks
- ✓ [The CHARM dosimetry document Link](#)
- ✓ Total integrated dose (TID): 56.9 Gy
- ✓ Total HEH fluence (cm<sup>-2</sup>): 1.62 e11
- ✓ Total ThN fluence (cm<sup>-2</sup>): 3.34 e11
- ✓ No latch-up has been seen on the entire electronics
- ✓ Expected #SEU in FPGA CRAM per minutes: **22.1**
- ✓ Expected #SEU in FPGA BRAM per minutes: **2.88**
- ✓ Rate of SEU detection and correction by SEM at configuration memory: **0.2 s<sup>-1</sup> (12 SEU per minute)**
- ✓ For the Link Boards, **failure is defined as link loss.**
- ✓ **The power cycling is used to failure recovery**
- ✓ MTBF of the Non-TMR firmware + SEM per Link: **250 minutes**
- ✓ MTBF of TMR firmware + SEM per link: **250 minutes**
- ✓ MTBF extended for HL-LHC condition:
- ✓  $MTBF_{HL-LHC} = 250 \text{ min} \times \frac{4.23 \times 10^5 \text{ (cm}^{-2} \text{ s}^{-1})}{1.8 \times 10^3 \text{ (cm}^{-2} \text{ s}^{-1})} = 40.79 \text{ days}$
- ✓ Redundant links make  $MTBF_{HL-LHC} \times 2$
- ✓ Power Recycling time: **5 sec**

- ✓ No over-current appeared during the test.
- ✓ No permanent damage nor performance degradation detected on the electronics.
- ✓ Electronics test results are fulfilled the HL-LHC requirement with following safety factors:

Item	CHARM	HL-LHC	Safety Factor
TID (Gy)	56.9	< 6	> 9.33
Total HEH fluence (cm <sup>-2</sup> )	1.62 × 10 <sup>11</sup>	< 2 × 10 <sup>10</sup>	> 8.1
Total ThN fluence (cm <sup>-2</sup> )	3.35 × 10 <sup>11</sup>	< 1.6 × 10 <sup>11</sup>	> 2
Irradiation Flux (cm <sup>-2</sup> s <sup>-1</sup> )	4.23 × 10 <sup>5</sup>	1.8 × 10 <sup>3</sup>	235
#SEU detection and Correction (minute <sup>-1</sup> )	12	0.14	85
#days between failure	0.17	40.79	
# failure per one HL-LHC year		2.45	
# failure in all HL-LHC years		24.5	
Dead time over HL-LHC (sec)		122.5	



# RPC Firmware Repository - GitLab

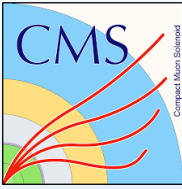


## • ***New Link system Firmware***

1. Unified Link Board
2. Unified Control Board
3. Control Board GTX IBERT test
4. Link System Irradiation
5. User Graphic Interface
6. TDC (1.56ns)
7. Diagnostic & Histogramming (LB)
8. GTX and LpGBT transceiver (Xilinx)
9. GTX Fixed Latency data transmission
10. FEB Controller
11. Multi Boot Remote Programming
12. Ethernet LAN
13. DDR3 interface Controller
14. Soft Error Mitigation Engine (SEM)
15. Front Panel Controller
16. TTC Clock Recovery & Phase Shift
17. Jitter Cleaner (State Machine Controller)
18. Control & Diagnostic (CB)
19. Slow Controller Emulator (SCE)
20. GBT-FPGA for the Control Board
21. Triple Modular Redundancy (TMR)

- [https://gitlab.cern.ch/cms\\_rpc\\_muons\\_firmware](https://gitlab.cern.ch/cms_rpc_muons_firmware)

The screenshot displays the GitLab repository structure for 'cms\_rpc\_muons\_firmware'. It shows a tree view under the 'Link System' group, which includes subgroups for 'Unified Link Board Firmware', 'Master Link Board', and 'Control Board GTX IBERT Test'. The 'Master Link Board' subgroup contains a project 'MLBv1'. The 'Control Board GTX IBERT Test' subgroup contains three projects: 'CB-IBERT only-bits', 'CB-IBERT 10.24 G', and 'CB-IBERT 4.8G'. The 'Unified Control Board Firmware' subgroup contains a project 'CBv1'. Each project entry shows its name, owner, and some statistics like stars and updates.



# Summary

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- Progress of the Link System Project is well advanced, and Prototypes are finalized.
- Each Board consumes 12 W. Still, there is room for power consumption reduction.
- The latest version of firmware is available on the RPC repository.
- The irradiation test of the Link System is completed, and the results are satisfactory.
- The electronics meet the HL-LHC radiation condition with high safety factors.
- No permanent damage nor performance degradation appeared on the electronics.
- Number of failures per board for 10 HL-LHC years is 24.5, which means 122.5-sec dead time over 10 HL-LHC years. The overall dead time for full system is 168560-sec.
- This number even would be better by using redundant links.
- The project schedule is protected with well enough floating time.



• **Thank you!**

# The CHARM Radiation Environment

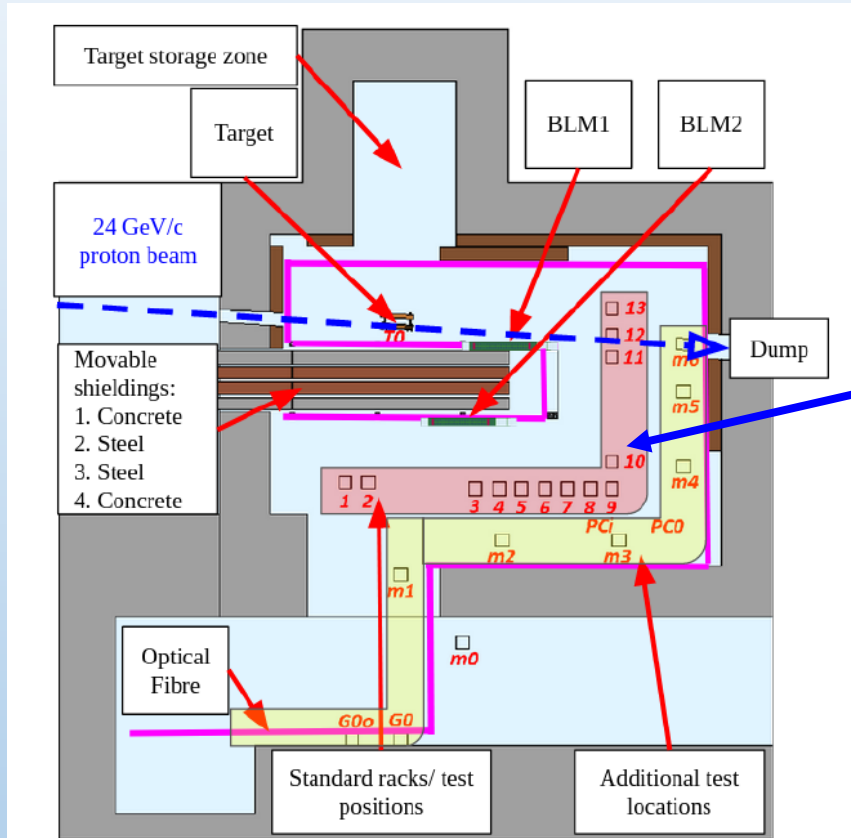
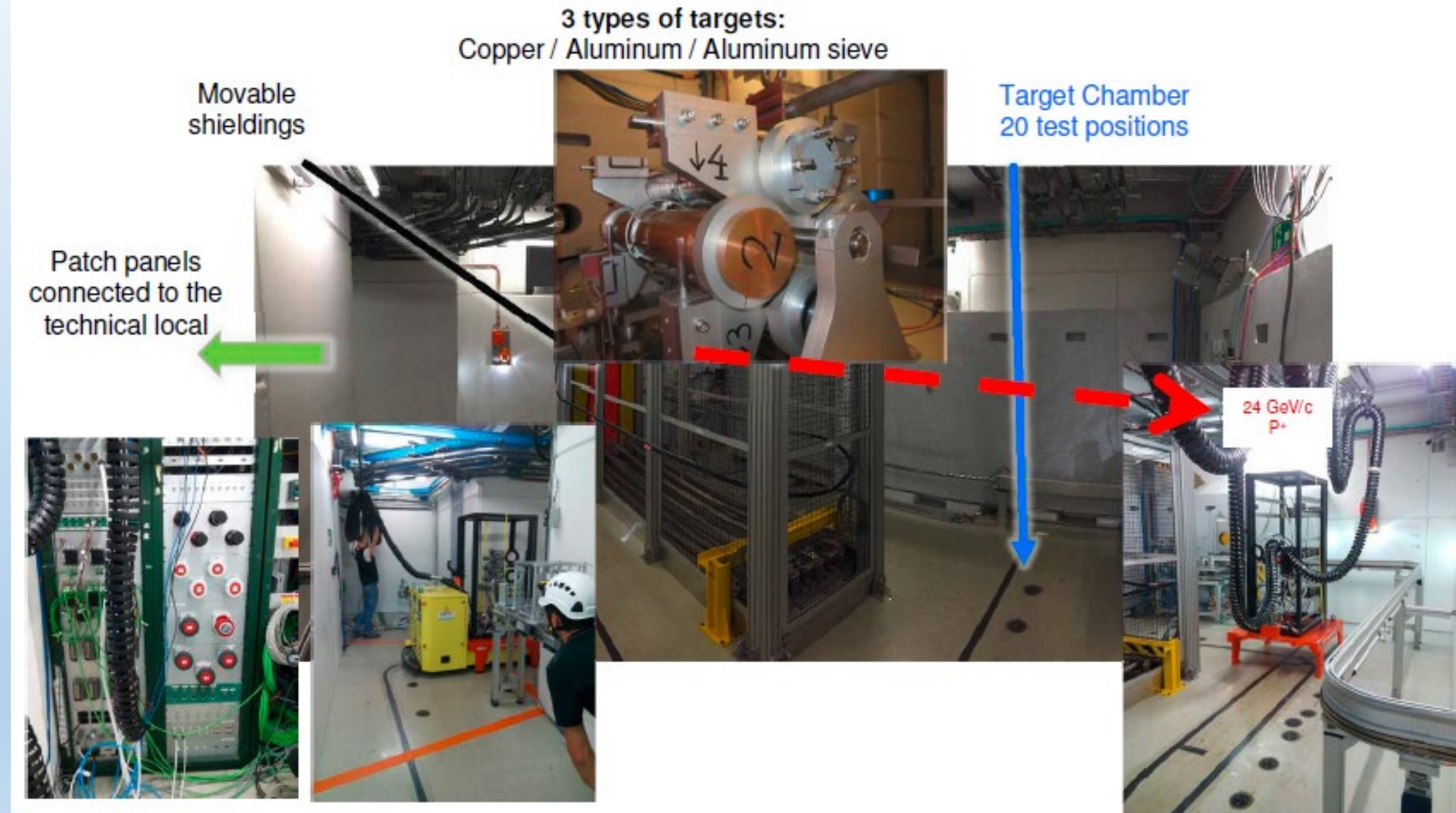


Fig. 1: Top view of FLUKA geometry of the CHARM test area. Two BLMs are installed at 1 m above beam height, one next to the target and one behind the movable shieldings. There

TABLE I: Maximum and weekly maximum integrated rates at CHARM for the Total Ionizing Dose, and the thermal neutron equivalent and high-energy hadron Fluences, obtained at the R10 location based on **FLUKA simulations**.

Quantity	Maximum Rate	Integrated Rate (per week)
<b>Total Ionizing Dose</b>	2.70 Gy/h	360 Gy
<b>Thermal neutron fluence</b>	$3 \times 10^6 \text{ cm}^{-2}\text{s}^{-1}$	$1.5 \times 10^{12} \text{ cm}^{-2}$
<b>High-energy hadron fluence</b>	$1.5 \times 10^6 \text{ cm}^{-2}\text{s}^{-1}$	$8 \times 10^{11} \text{ cm}^{-2}$

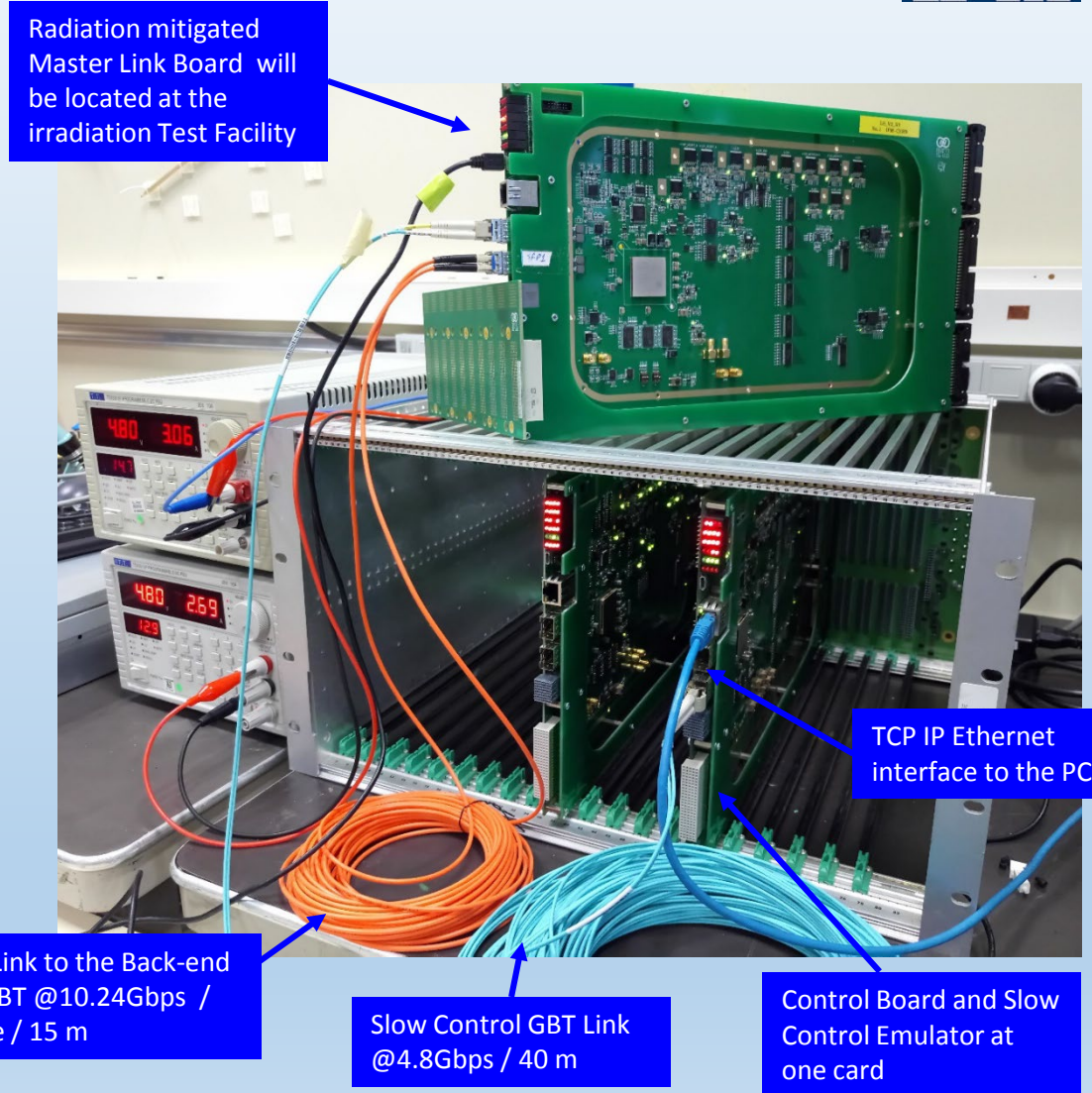
# The CHARM Irradiation Area I



# Preparation for Irradiation test in Cern 904 Lab

## □ June/July 2022: Preparation for Irradiation Test

- ✓ Link System Test Setup was tested at 904 Lab.
- ✓ System fully stable, responsive during 8 hours continuous run.
- ✓ Cold Test was passed. Error injection to the FPGA was done and every errors (virtual SEU) were detected and corrected by FPGA SEM IP core.



Radiation mitigated Master Link Board will be located at the irradiation Test Facility

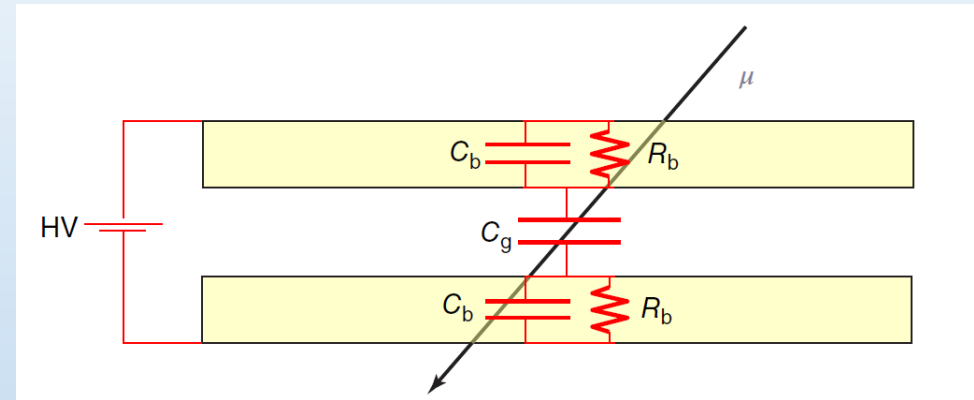
TCP IP Ethernet interface to the PC

Muon hit data Link to the Back-end electronics LpGBT @10.24Gbps / Loopback Mode / 15 m

Slow Control GBT Link @4.8Gbps / 40 m

Control Board and Slow Control Emulator at one card

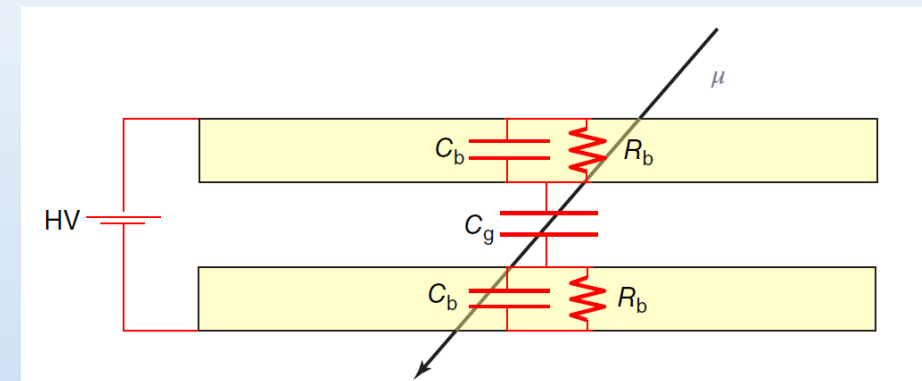
- Simplified circuit for an RPC with resistive electrodes.
- $C_b$  and  $C_g$  represent the capacitance of each electrode plate and of the gas gap, respectively;
- $R_b$  represents the resistance of the electrode plates.
- The gas is not ionized. In this “static” situation, the applied voltage HV is correspondingly transferred to the gas gap, and no current is flowing through the circuit.
- The gas is crossed by an ionizing particle.
- In this case, the related discharge can be modeled as a current generator, which discharges the capacitor  $C_g$  (associated to the gas gap) in such a way that the voltage initially applied to the gas is transferred to the resistive electrodes (described by the capacity  $C_b$  and, as already pointed out, by the resistance  $R_b$ ). The system comes back to the initial configuration following an exponential law, with a characteristic time constant  $\tau$  given by:



$$\tau = 2R_b \left( \frac{C_b}{2} + C_g \right) = 2\rho_b \frac{d}{S} \left( \frac{1}{2} \epsilon_0 \epsilon_r \frac{S}{d} + \epsilon_0 \frac{S}{g} \right) = \rho_b \epsilon_0 \left( \epsilon_r + 2 \frac{d}{g} \right)$$

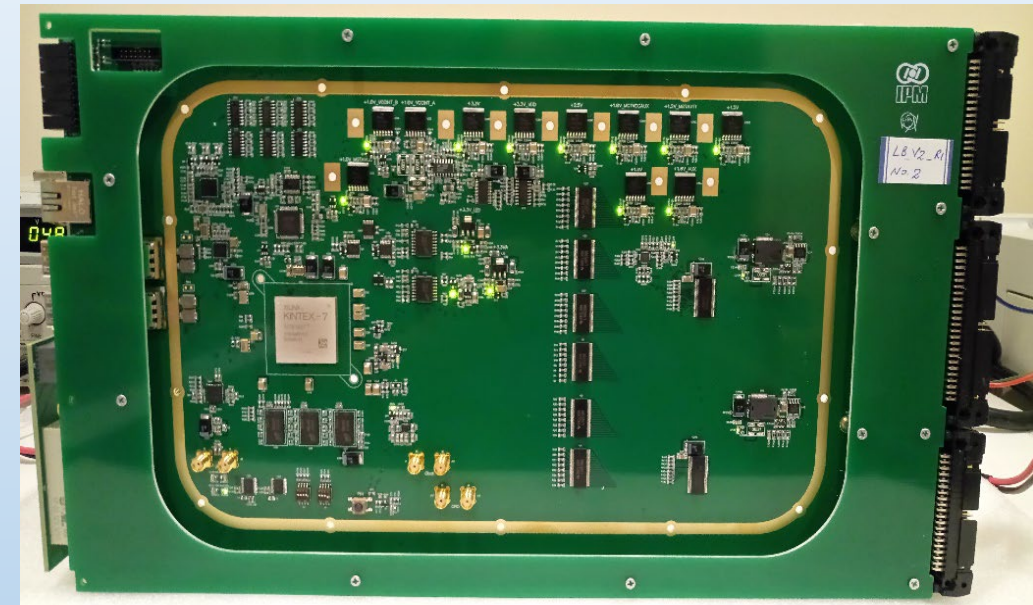
- $\epsilon_r$  is the relative dielectric constant of the electrode material,
- $\rho_b$  its resistivity,
- $\epsilon_0$  is the dielectric constant of the vacuum,
- $g$  is the gas gap thickness,
- $d$  is the thickness of the electrodes, and
- $S$  is the electrode surface considered.

Note that  $\tau$  does not depend on the dimension  $S$  of the zone considered on the electrode.  
 The spark quenching effect is stronger when  $C_b$  is small, so the thickness of the anode plate and its dielectric constant play an important role.

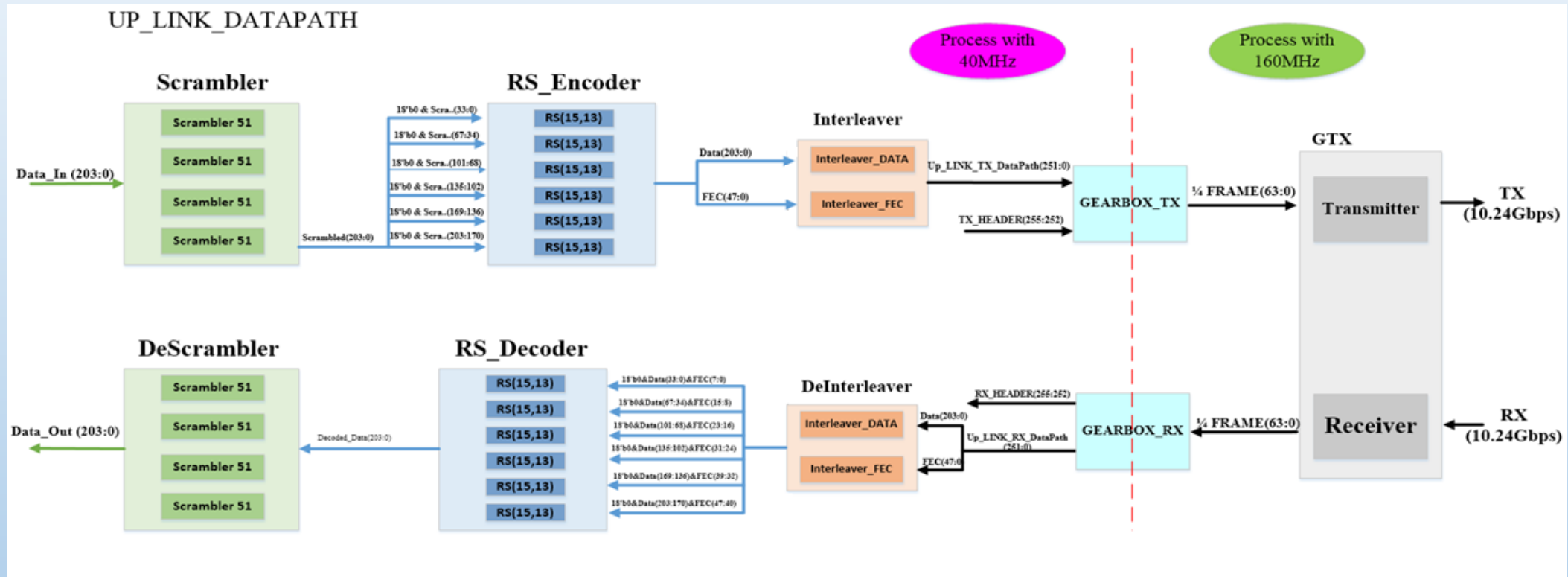


- $\rho_b = 10^{11} \Omega\text{cm}$  typical **avalanche** or **discharge durations** which are on the order of  $10 \text{ ns} \ll \tau$ .
- In this time interval, the electrodes behave as perfect dielectric materials; in other words, they are perfect insulators, and therefore the voltage across the gas gap is very low and the discharge inside the gas cannot be sustained.
- This is the **auto quenching** mechanism at the base of the operation of this detector.

1. 14 Layers PCB – FR4
2. 96 Input Channels. 15 kV ESD protected.
3. Twenty-four output channels to inject a signal in the FEB(s) for calibration, a test of the flat cables and connectors.
4. Detector Diagnostic and monitoring:
  - a. Full/Adjustable window Histograms
  - b. RPC Data logging
  - c. Timing Histogram
5. Muon Hit time information with a time resolution of 1.5 ns.
6. Collects 42 hits per Bunch Crossing without any buffer overflow and data loss.
7. Transmit 18 hits per Bunch, Crossing to the L1T through a 10 G optical Link.



## • Transceiver Architecture

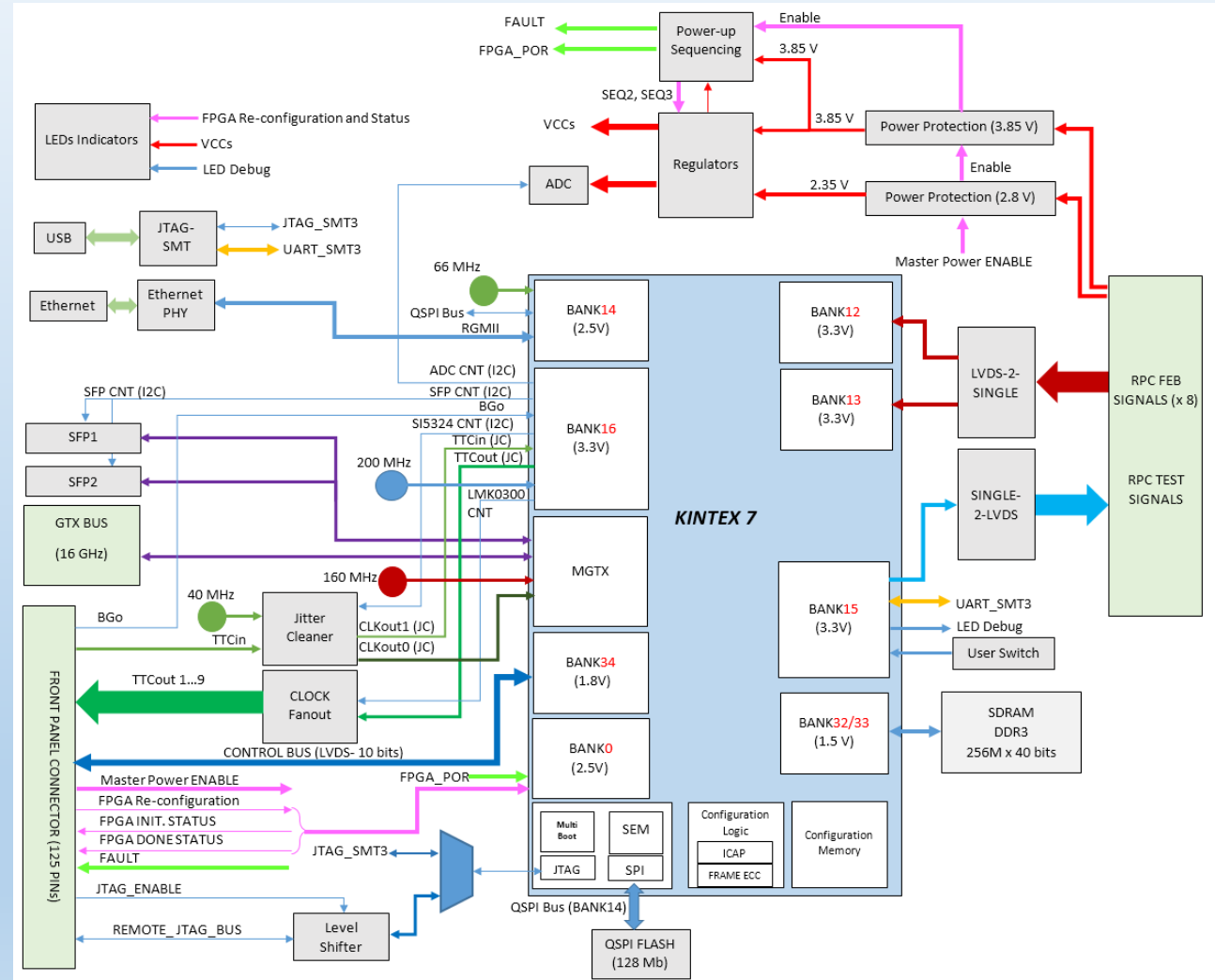


- ✓ In the scrambler avoiding long sequences of bits of the same level helps GTX distinguish each bit's boundary.
- ✓ Using Reed-Solomon, by adding redundancy to each packet, will have the possibility to correct defects.
- ✓ Using Interleaver by distributing defects in a frame makes FEC more robust.

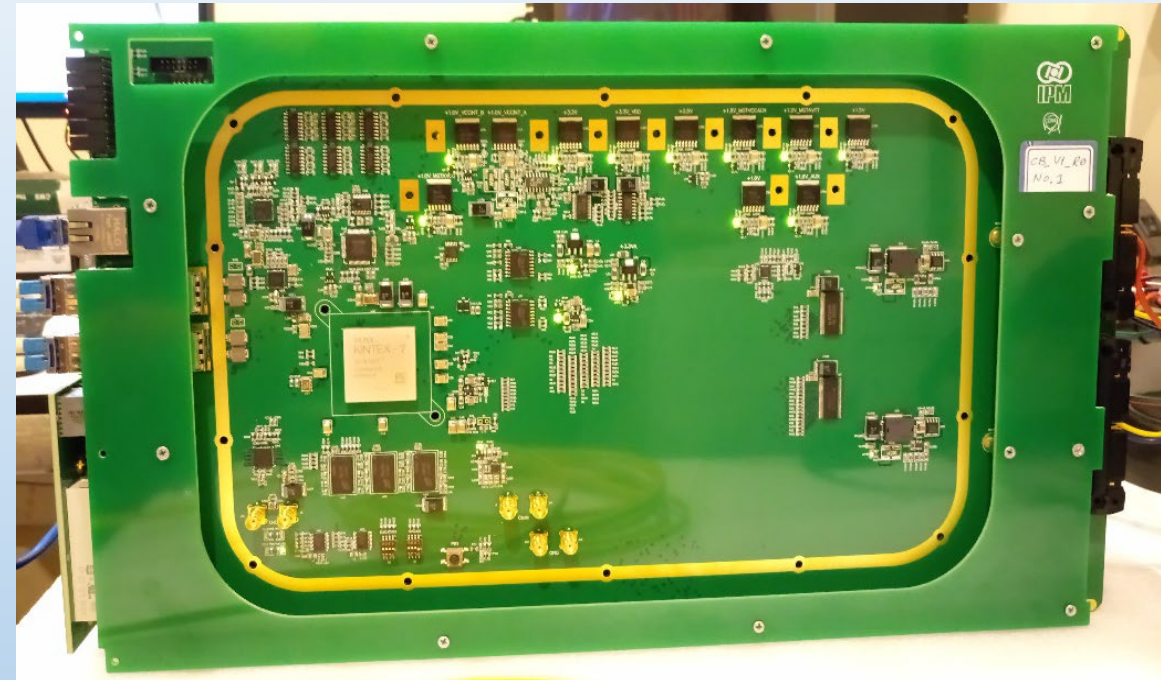
# New Link Board Hardware Architecture

- The design specifications and components:

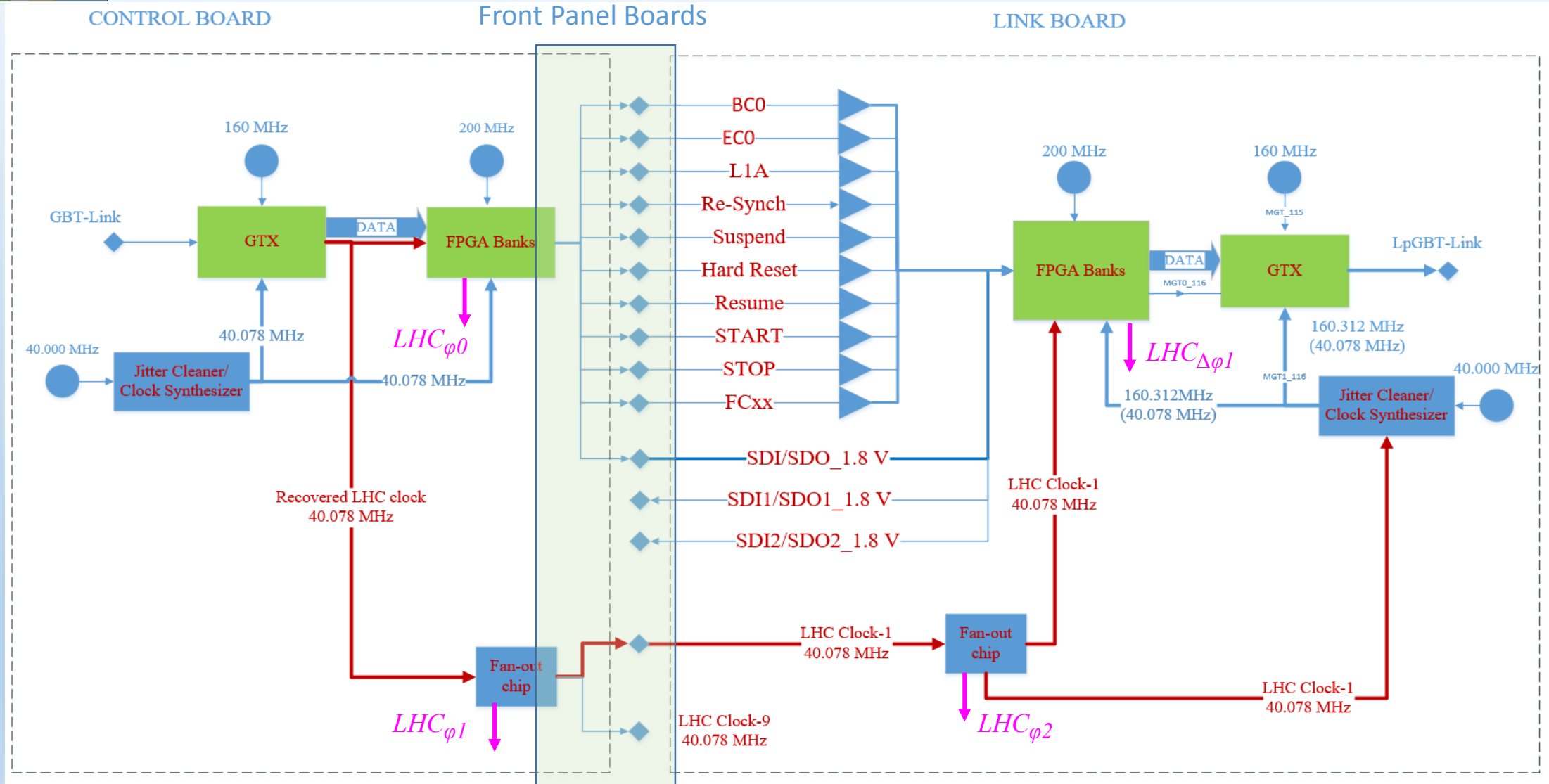
- FPGAs are KINTEX7, XC7K160T-2FFG676I.
- Fully support **10.3 Gbps** data transmission. FPGA Chip is equipped with a heat sink.
- High-resolution TDCs (at the steps of **1.56 ns**) implemented into the Kintex7 FPGA
- Two Redundant optical data transmission lines at the data rate of **10.24 Gbps**
- Ethernet link for the debugging and onboard JTAG programmer
- 256 M x 40 bits of SDRAM-DDR3 for data buffering and debugging
- Data transmission with adjacent slave link boards through the SAMTEC back-plane type connector with a bandwidth of **16 GHz** and front panel PCB board.
- Radiation Mitigation is based on Triple Modular Redundancy (TMR) techniques and **Soft Error Mitigation (SEM) IP core** from Xilinx.
- Voltage Regulators selected from low dropout linear regulator families have already been tested under radiation.



- 14 Layers PCB – FR4
- The only bridge between RPC backend electronics and Link Boards
- Optical Links to receive TTC, Fast, and Slow commands. GBT-FPGA link driver.
- TTC clock and Fast BGo commands, BC0
- TTC Clock Phase shift adjustment
- FEB Parameter Configuration and Verification.
- Control and monitor the Link Boards  
Histograms, Data Logs, and Diagnostics through the front panel bus.

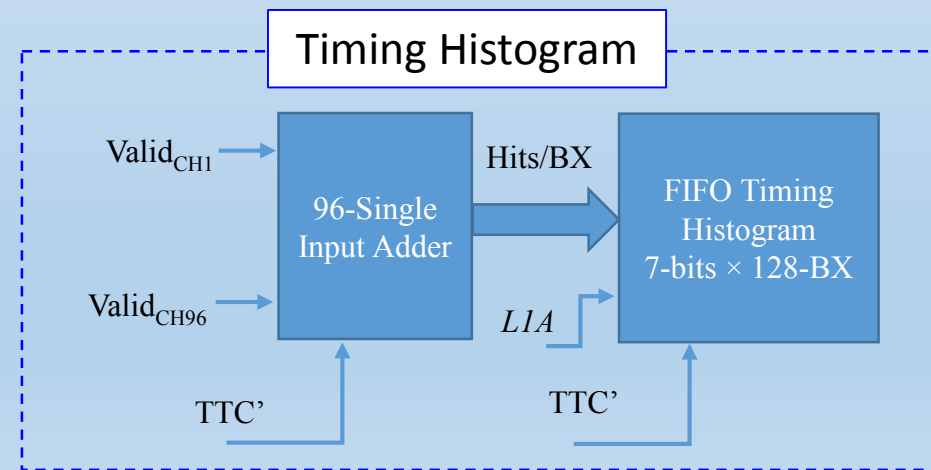
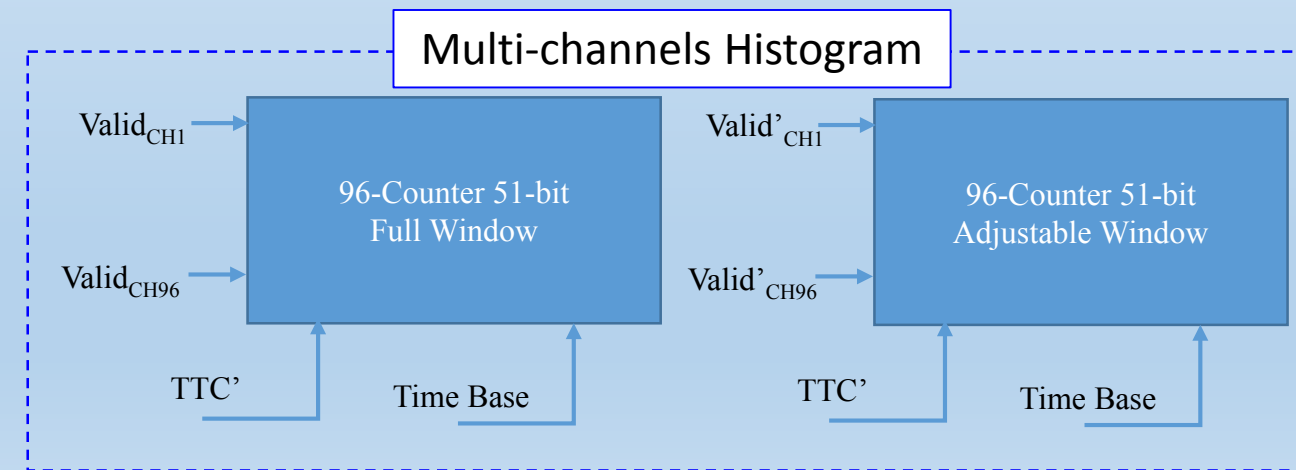
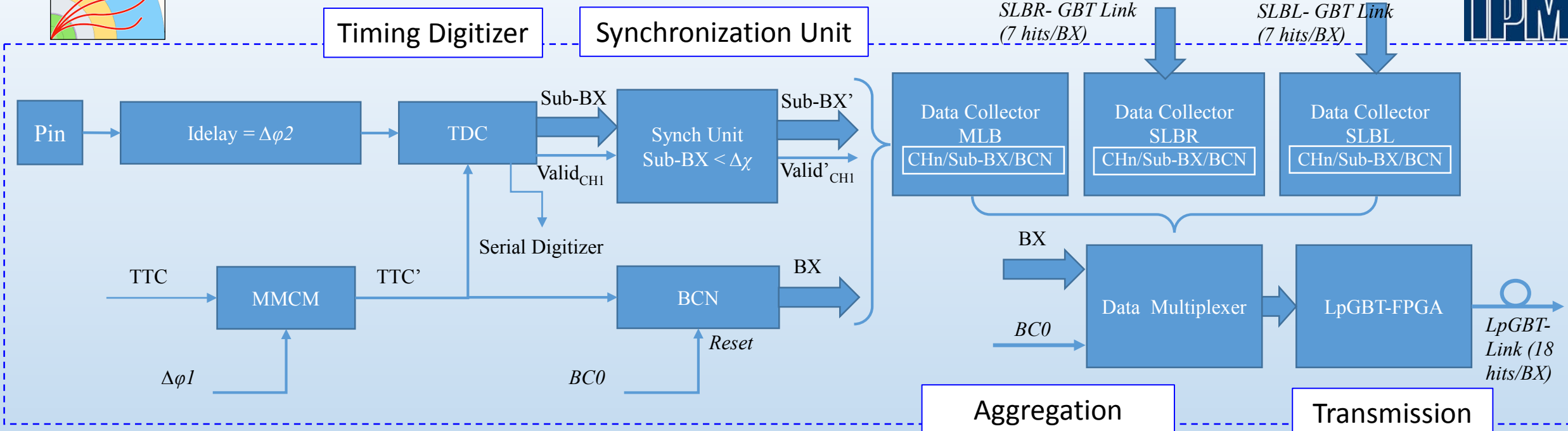


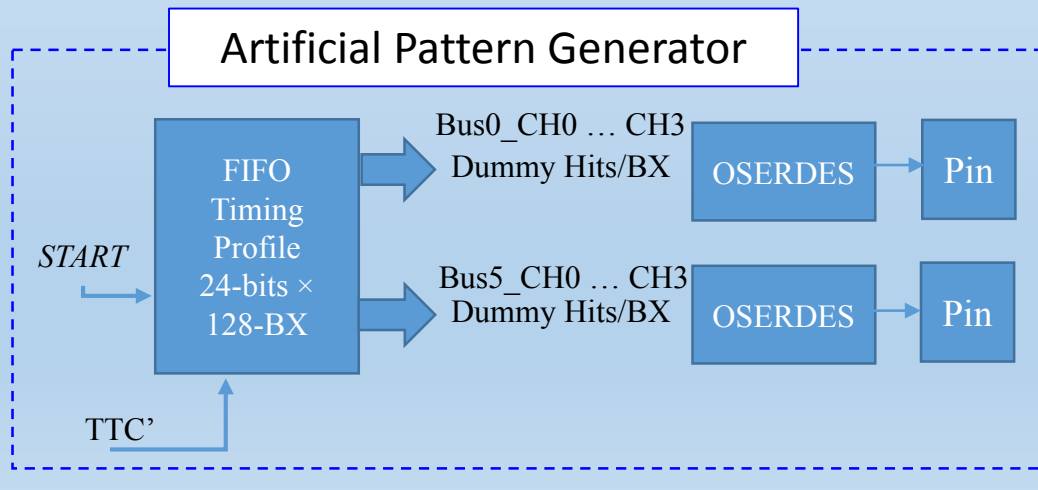
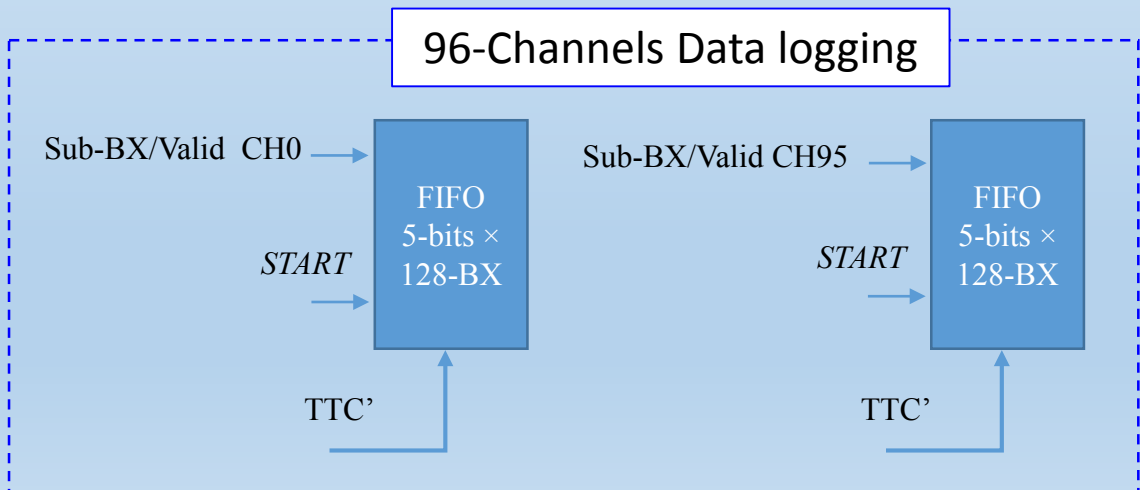
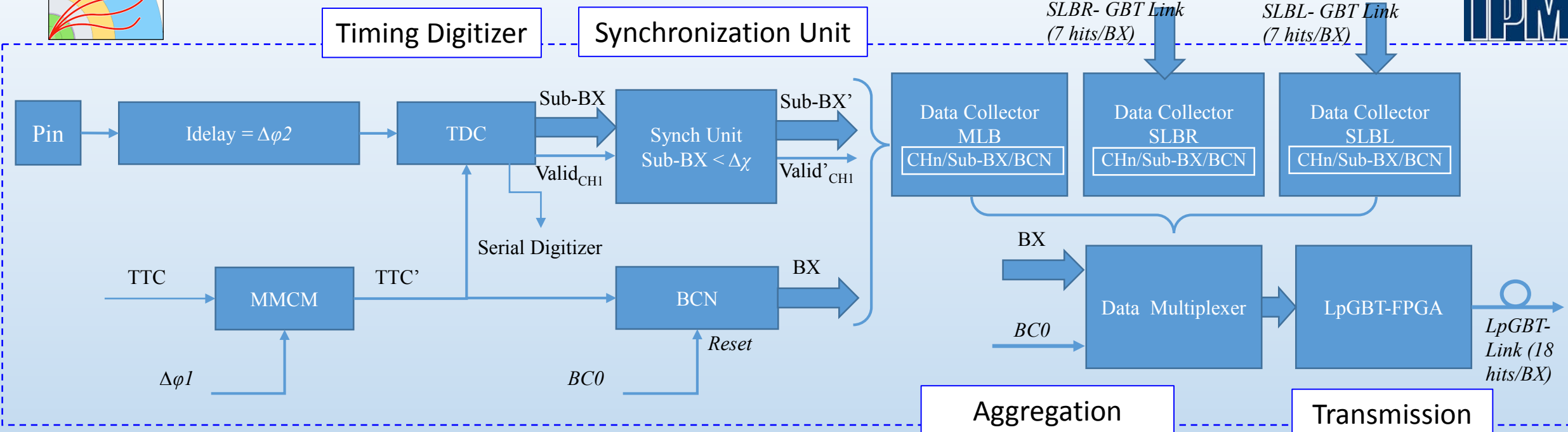
# Link System Clock distribution Scheme





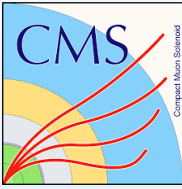
# RPC data processing - RPC signal time tagging





# **Phase-2 RPC Link System**

## **Electronics Radiation Hardness**

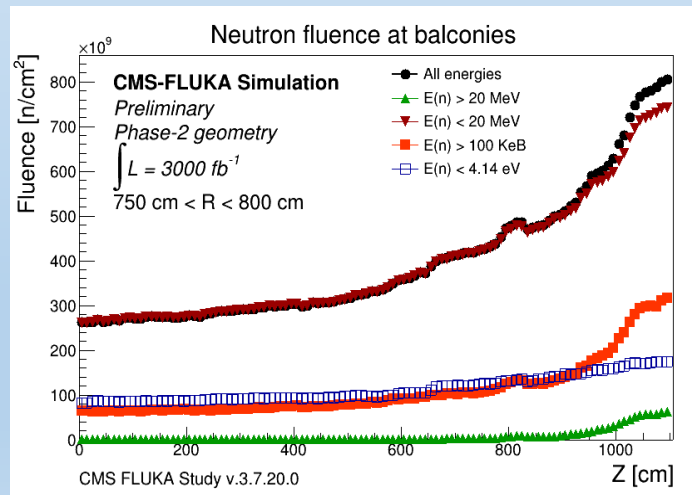
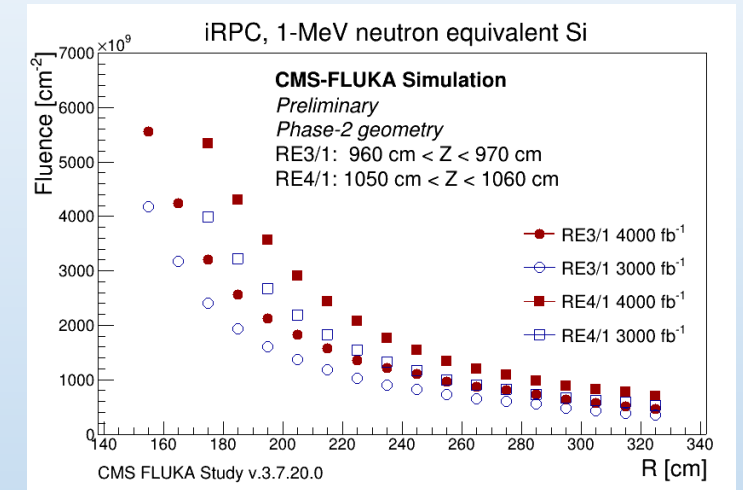
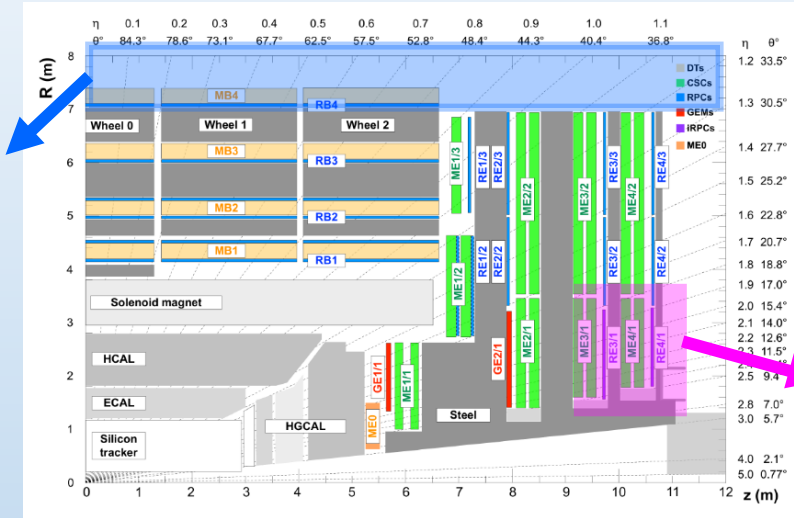
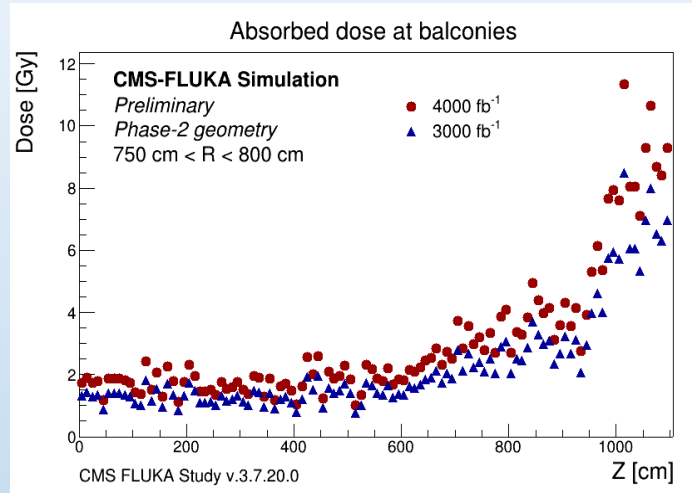


# Technical aspect of Radiation Test

- Outline

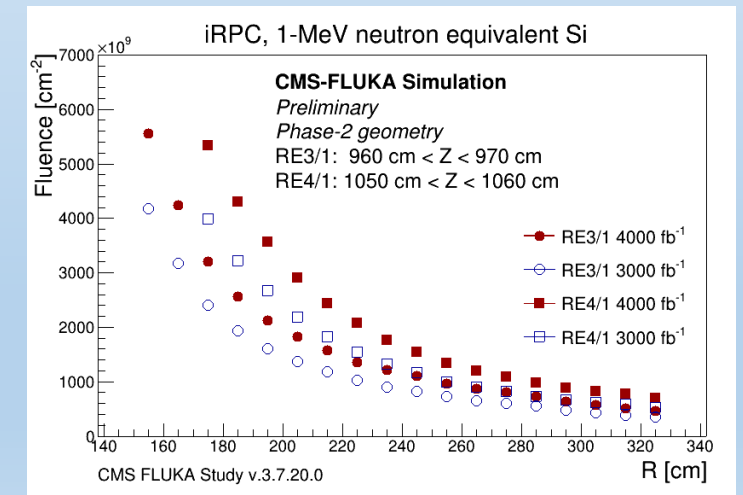
- Radiation Effects on Electronics (Pages 4, 5,6)
- Tests Standards and Guidelines (Pages 7, 8)
- Electronics Validation Strategy (Page 9)
- Goals (Page 10)
- How measure the Single Event Effects (Page 11)
- Which type of beam? (Page 11)
- **Neutron** beam or **Proton** beam or **Both**?
- Plan
- Where?
- When ?
- Procedure?
- Logistics

# Expected Fluence and Dose at HL-LHC



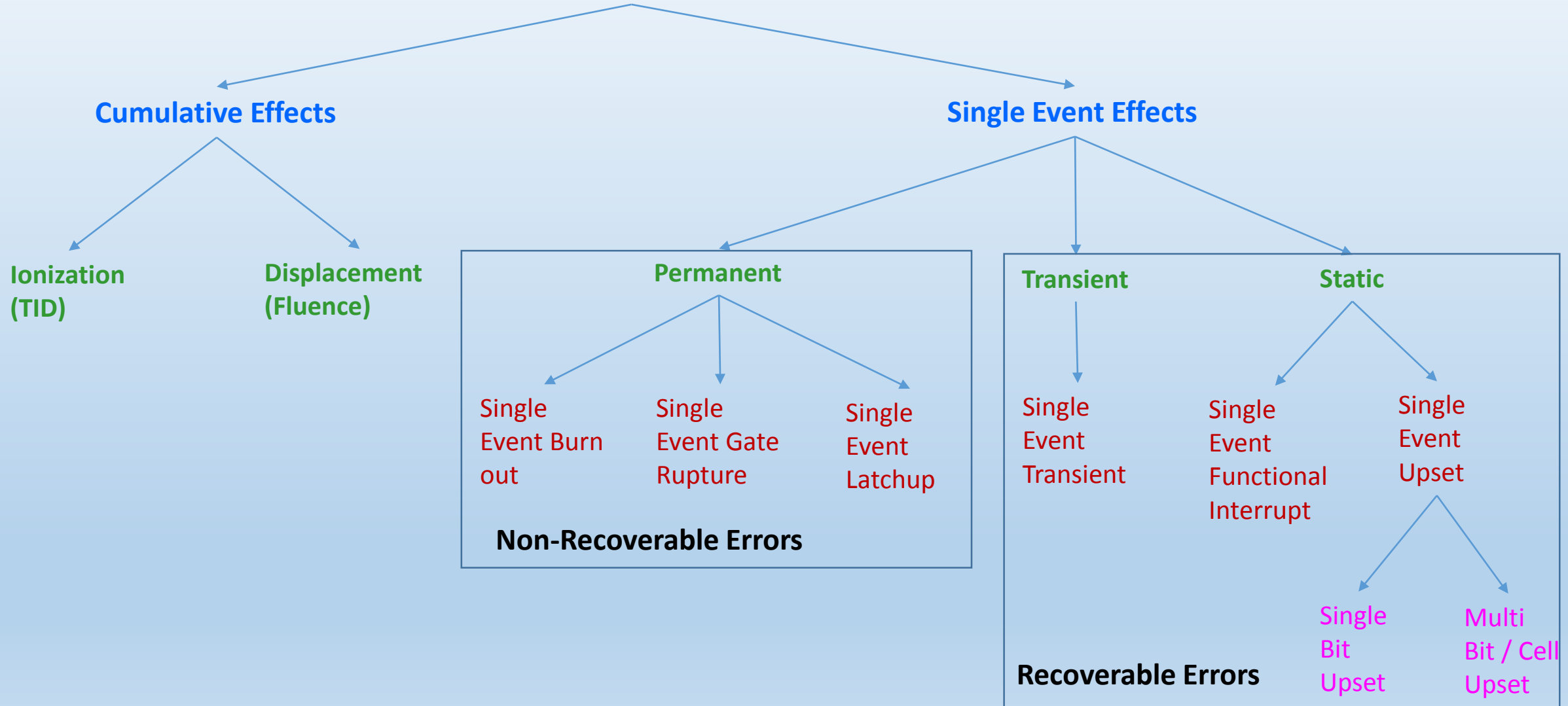
- **Expected fluence and dose (RE34/1 FEBs)**
  - at R=303 cm for RE3/1 is **~4.3 (5.8) × 10<sup>11</sup> n/cm<sup>2</sup>**, and
  - at R=304 cm for RE4/1 it is about **6.2 (8.2) × 10<sup>11</sup> n/cm<sup>2</sup>**,
  - at R=303 cm for RE3/1 is **~10 (13.6) Gy**
  - at R=304 cm for RE4/1 it is about **18 (24) Gy**
  - where R=303 (304)cm are the expected FEB positions

- **Expected fluence and dose (Balcony)**
  - The total irradiation fluence **800 × 10<sup>9</sup> cm<sup>-2</sup>**
  - Maximum integrated dose is about **10 Gy**



# Radiation Effects in Electronics

## Radiation Effects





# Radiation Hardness of Electronics for Phase-2 Upgrade



## • Simulation of the CMS Radiation environment

- Maximum expected Fluence after collecting 3000 fb<sup>-1</sup>
- The expected absorbed dose after collecting 3000 (4000)fb<sup>-1</sup>
- NO Safety Factor

## • Radiation could cause

- Permanent damage
- Temporary effects such as data corruption induced by SEU

## • Electronics

- Digital Components: TID/displacement damage, SEU, Latchup  $E_n < 20 \text{ MeV}$
- Analog Components: TID/displacement damage,  $E_n < 1 \text{ MeV}$  [1]

## • Goals:

- Obtain the SEU cross section of FPGA resources (Configuration Memory, BRAM, MGTs, FFs)
- Estimate of the Upset rate within the CMS radiation environment
- Digital/Analog Components : Check the fault resilience of the other ASICs
- Evaluation of the rad-hard techniques adopted during the experiments must prevent build up of errors in different FPGA parts

	Fluence [particles cm-2]	Dose [Gy]
<b>FEB for RE3/1 (R = 304 cm)</b> near to the border at higher radii	<b>Max = <math>4.3 \times 10^{11}</math></b> <b>1-MeV NE in SI</b>	<b>Max = 10</b> <b>(13.6)</b>
<b>FEB for RE4/1 (R = 304 cm)</b> near to the border at higher radii	<b>Max = <math>6.2 \times 10^{11}</math></b> <b>1-MeV NE in SI</b>	<b>Max = 18 (24)</b>
<b>Link board for Barrel (Z &lt; 600 cm)</b>	<b>Max = <math>350 \times 10^9</math></b> <b>Neutrons with <math>E_n &lt; 20 \text{ MeV}</math></b>	<b>Max = 2</b>
<b>Link board for Endcap (Z &gt; 600 cm)</b>	<b>Max = <math>800 \times 10^9</math></b> <b>Neutrons with <math>E_n &lt; 20 \text{ MeV}</math></b>	<b>Max = 10</b>

## Single Event Effects

Table 1. Non destructive SEE phenomena.

Upset - SEU <sup>1</sup>	corruption of the information stored in a memory element	Memories, latches in logic devices
Multiple Bit Upset - MBU	several memory elements corrupted by a single strike	Memories, latches in logic devices
Functional Interrupt -SEFI	loss of normal operation	Complex dev. with built-in state/control section
Transient - SET	impulse response of certain amplitude and duration	Analog and Mixed Signal circuits, Photonics
Disturb - SED	momentary corruption of the information stored in a bit	combinational logic, latches in logic devices
Hard Error - SHE	unalterable change of state in a memory element	Memories, latches in logic devices

Table 2. Destructive SEE phenomena.

Latchup - SEL	high-current conditions	CMOS, BiCMOS devices
Snapback - SESB	high-current conditions	N- MOSFET, SOI devices
Burnout - SEB	destructive burnout	BJT, N-channel Power MOSFET
Gate Rupture - SEGR	rupture of gate dielectric	Power MOSFETs
Dielectric Rupture - SEDR	rupture of dielectric	Non-volatile NMOS struct., FPGA, linear devices...

## Cumulative Effects

Table 3. Typical TiD degradation modes in devices.<sup>2</sup>

<i>device</i>	<i>Degradation mode</i>
MOS	Shifting of threshold voltage
BJT	Current gain degradation
Digital circuits	Increased leakage current (Iccop, Icc-sb), reduced retention time (DRAMs and SDRAMs)
Linear devices	Increased Offset voltage and bias current

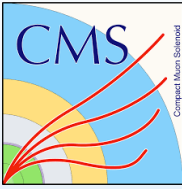
Table 4. Typical DD degradation modes in circuits.

<i>device</i>	<i>Degradation mode</i>
CCD/APS	Reduced responsivity (Increase of dark current, RTS occurrence... <sup>o</sup> )
Bipolar Linear devices	Gain degradation
Solar cells	Reduced efficiency (output power, short circuit current)
Laser diode	Threshold current increase

Reference: R. Velazco et al. (eds.), *Radiation Effects on Embedded Systems*, 201–251. © 2007 Springer.

- Two main standards are widely used within the framework of **SEE testing**:
  - 1) **ESA/SCC 25100**: Single Event effects test methods and guidelines
  - 2) **JEDEC JESD57**: Test procedures for the measurement of Single-Event Effects in semiconductor devices from heavy ion irradiation
  
- The SCC standard applies to proton and heavy ion testing whereas the JEDEC standard only addresses heavy ion testing.

Requirements	ESA/SCC 25100	JEDEC JESD57
Scope	Single Event effects test method and guidelines	Test procedures for the measurement of Single-Event Effects in semiconductor devices from <b>heavy ion</b> irradiation
Radiation sources and characteristics	HI : range $\geq 30\mu\text{m}$ , $10^2 \geq \text{Flux} \geq 10^5 \text{ ions/cm}^2.\text{s}$ p+ : 20-300 MeV $10^5 \geq \text{Flux} \geq 10^8 \text{ ions/cm}^2.\text{s}$	range large compared to the depth of the collection region, $10^2 \geq \text{Flux} \geq 10^5 \text{ ions/cm}^2.\text{s}$ LET up to 120 MeV/mg.cm <sup>2</sup>
Dosimetry	Uniformity $\pm 10\%$ over the device area Flux $\pm 10\%$	Energy $\pm 10\%$ Uniformity $\pm 10\%$ over the device area Flux $\pm 10\%$
Testing requirements	Sample size $\geq 3$ (same dtc) 5 measurements at different effective LETs (HI) or Energies (p+, normal incidence) Max fluence of resp. $10^7$ and $10^{10}$ part./cm <sup>2</sup> .s for HI and p+ or a meaningful number of events	Measurements at onset threshold, 10%, 25%, 50% and 75-80% of the saturated $\sigma$ , Max fluence of $10^7 \text{ ions/cm}^2.\text{s}$ for “hard” devices, $10^6 \text{ ions/cm}^2.\text{s}$ or 100 events whichever comes first for “soft” devices Tilt angles limited to 60°



# Main features of TID radiation types.



- Radioactive Cs137 and Co60 sources deliver gamma rays, two strong advantages:
  - the very wide range of dose rates available
  - the fact that the total dose is well controlled in the device thickness.
- As photons delivered by Co60 have a large energy, 1.17 and 1.33 MeV, dose uniformity is ensured.
- This advantage can be lost if the irradiation facility is not correctly filtered and delivers a sizeable ratio of low energy scattered photons inducing dose enhancements. Consequently, it is necessary to take care to correctly assess accurate dosimetry and use adequate filtering methods.

Radiation type	Main advantages	Main drawbacks
Electrons (accelerator)	High dose rate available Representative of some orbits	Costly Not adequate for low dose rates
Protons (accelerator)	High dose rate available Representative of some orbits	DD contribution Costly
X rays (photons)	High dose rates available Low cost	Dose enhancement effect Not adequate for low dose rates
Cs <sup>137</sup> & Co <sup>60</sup> sources (gamma rays)	Very large dose rate range Dose uniformity	Heavy shielding necessary Non-dominant in orbit

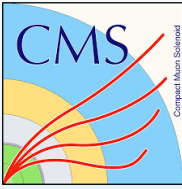


# Electronics validation Strategy



Step	Description	FPGA	ASIC	Goals
1	<b>Obtain</b> the SEU cross section of FPGA resources (Configuration Memory, BRAM, MGTs, FFs)	<ul style="list-style-type: none"> <li>✓ <math>\sigma_{\text{CRAM}}: 6.89 \times 10^{-15} \text{ (cm}^2\text{/bit)}</math></li> <li>✓ <math>\sigma_{\text{BRAM}}: 6.15 \times 10^{-15} \text{ (cm}^2\text{/bit)}</math></li> <li>✓ <math>\sigma_{\text{GTX}}: 7.27 \times 10^{-12} \text{ (errors/lane/cm}^2\text{/bit)}</math></li> </ul>	-	
2	<b>Estimate</b> of the Upset rate within the CMS radiation environment	✓	-	
3	<b>Cold-Test, Fault injection in Lab and</b>	✓ Firmware mitigation will be started after completion of the firmware integration	-	<ul style="list-style-type: none"> <li><input type="checkbox"/> Evaluation of the rad-hard techniques</li> </ul>
4	<b>Hot-Test, (SEE)</b>	✓ Proton Beam / Heavy Ion cocktail	-	<ul style="list-style-type: none"> <li><input type="checkbox"/> Evaluation of the rad-hard techniques adopted during the experiments must prevent build up of errors in different FPGA parts</li> <li><input type="checkbox"/> Irradiations are done in vacuum and for most of the ions naked chips are needed.</li> </ul>
5	<b>Full Electronics Test (TID)</b>	<ul style="list-style-type: none"> <li>✓ 300 krad</li> <li>✓ <math>1.3 \times 10^{13} \text{ (proton/cm}^2\text{) without TIFR}</math></li> </ul>	<ul style="list-style-type: none"> <li>✓ Cobalt-60 or X-Ray</li> </ul>	<ul style="list-style-type: none"> <li><input type="checkbox"/> Check the fault resilience of all electronics active devices such as FPGA, Digital and Analog ASICs, under X-Ray at 1 MeV Neutron Equivalent energy. <b>Exactly similar to Medical irradiation treatment.</b></li> </ul>

[1] Radiation testing campaign results for understanding the suitability of FPGAs in detector electronics, [10.1016/j.nima.2015.11.033](https://doi.org/10.1016/j.nima.2015.11.033), 2015.



# Goals of the SEE Experiment

## ➤ A SEE experiment aims

- ✓ evaluating in real-time the device's response under consecutive exposures with several beam characteristics.

## ➤ The final objective

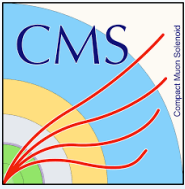
- ✓ is to obtain a good description of the device behavior and an accurate measurement of its radiation response ( $\sigma(E)$  or  $\sigma(LET)$  for each error mode) to enable the calculation of reliable in-flight SEE rates.

# How to measure the SEE

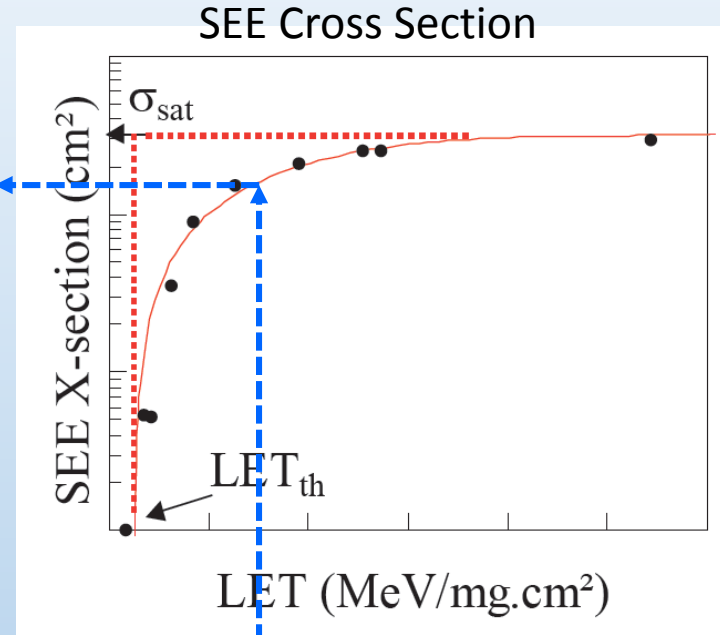
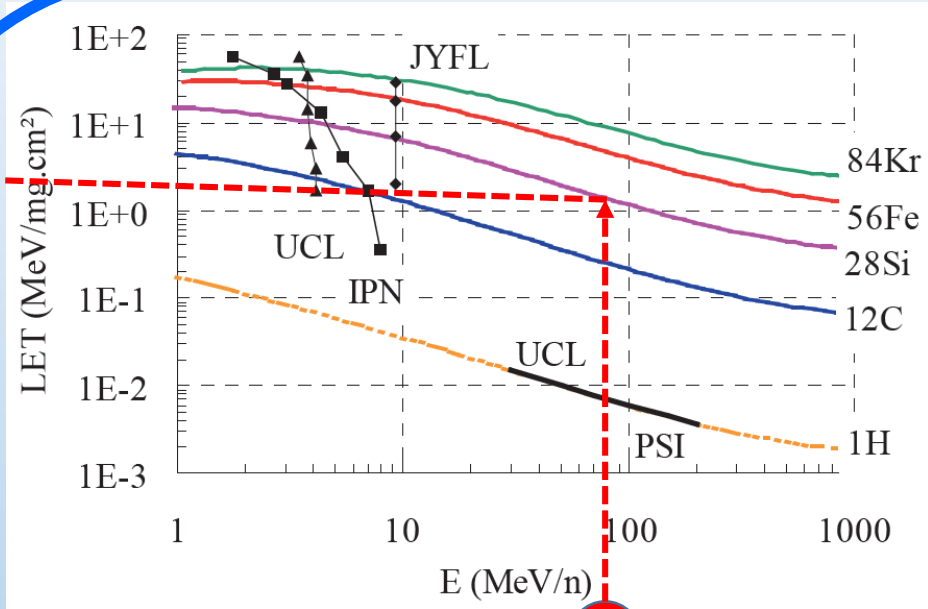
- $\sigma (\text{LET}) = \frac{\text{Number of SEE}}{\text{Fluence}}$  (units in  $\text{cm}^2$ )
- $\text{LET} (\theta) = \text{LET} (0^\circ) / \cos \theta$

- $\text{Number of SEUs} = \text{Fluence} \times \sigma (\text{LET})$

- $\sigma (\text{LET})$  Correlated with LET
- LET Correlated with Particle or Ion beam Energy and Atomic mass of target material



# Linear Energy Transfer (LET)



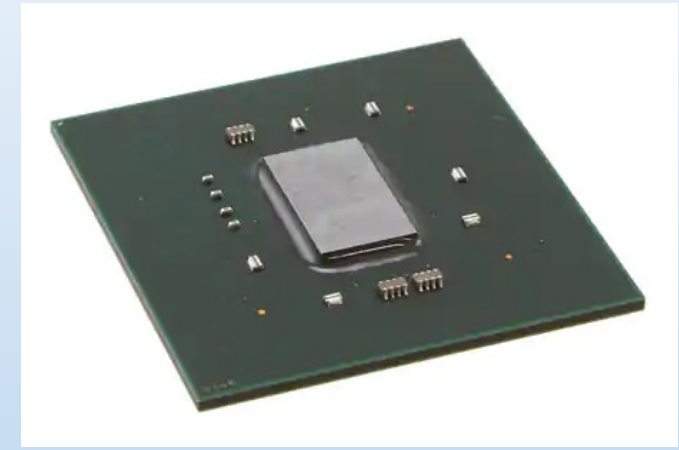
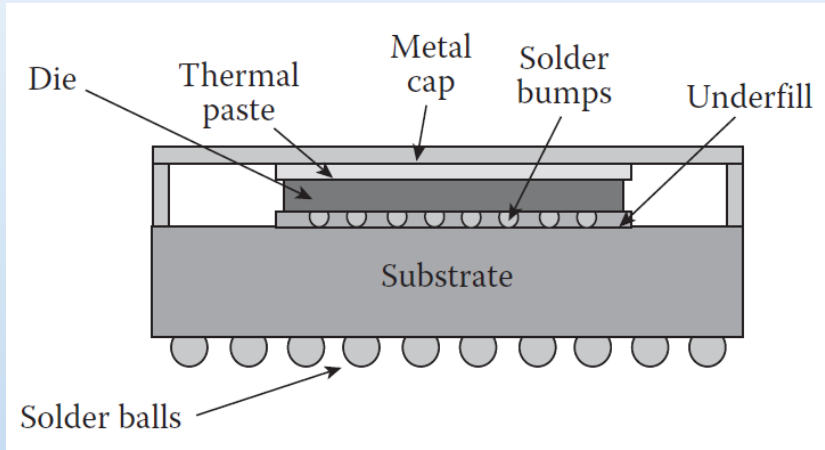
30 MeV proton beam  $\rightarrow$  LET  $1.469 \times 10^{-2}$  MeV cm<sup>2</sup> mg<sup>-1</sup>

$$t_{HL-LHC} = \frac{3000 \times 10^{39} \text{ cm}^{-2}}{1.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}} = 2.0 \times 10^8 \text{ s}$$

$$\sigma(\text{LET}) = \frac{\text{Number of Events}}{\text{Fluence}} \quad (\text{units in cm}^2)$$

$$\text{LET}(\theta) = \text{LET}(0^\circ) / \cos \theta$$

# Kintex7 Flip-chip Package



➤ Schematics of a flip-chip metallic package

➤ Link and Control Board Kintex-7 FPGA Flip-chip metallic Package

➤ Kintex-7 K160T Die after removing metal cap

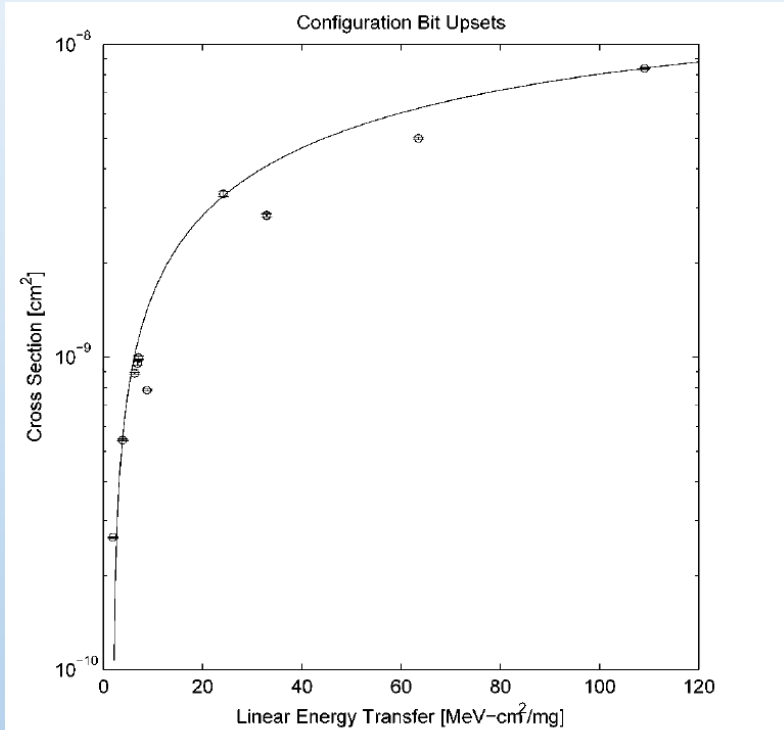


Fig. 1. Weibull curve for configuration memory cell upsets.  $L_{th}=1.9$  [MeV-cm<sup>2</sup>/mg],  $\sigma_{sat}=1.43e-8$  [cm<sup>2</sup>/bit],  $W=125.3$  [MeV-cm<sup>2</sup>/mg],  $S=0.78$ .

**Mitigation Technique:**  
Scrubbing

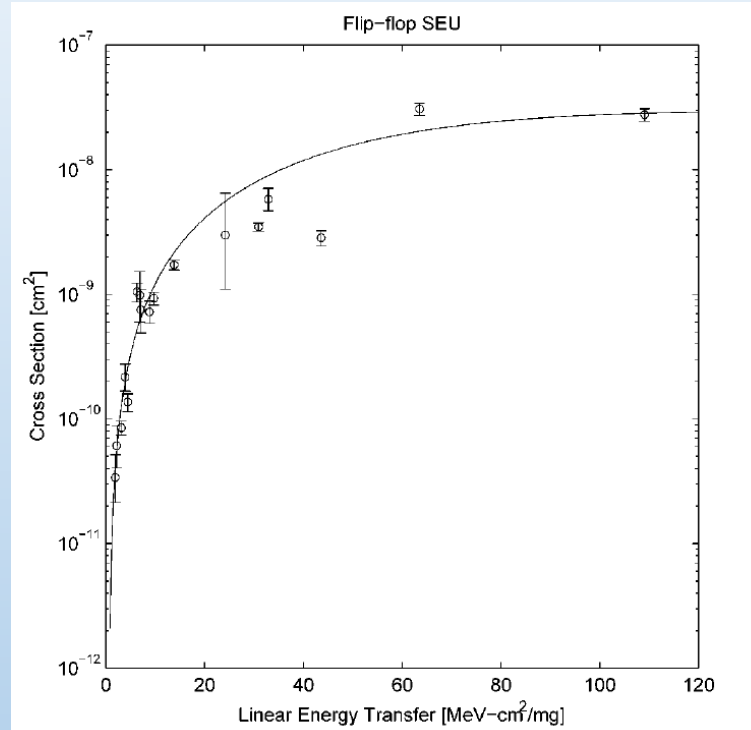


Fig. 3. Flip-flop memory cell SEU event Weibull curve.  $L_{th}=0.6$  [MeV-cm<sup>2</sup>/mg],  $\sigma_{sat}=3.0e-8$  [cm<sup>2</sup>/bit],  $W=58.4$  [MeV-cm<sup>2</sup>/mg],  $S=1.74$ .

**Mitigation Technique:**  
TMR

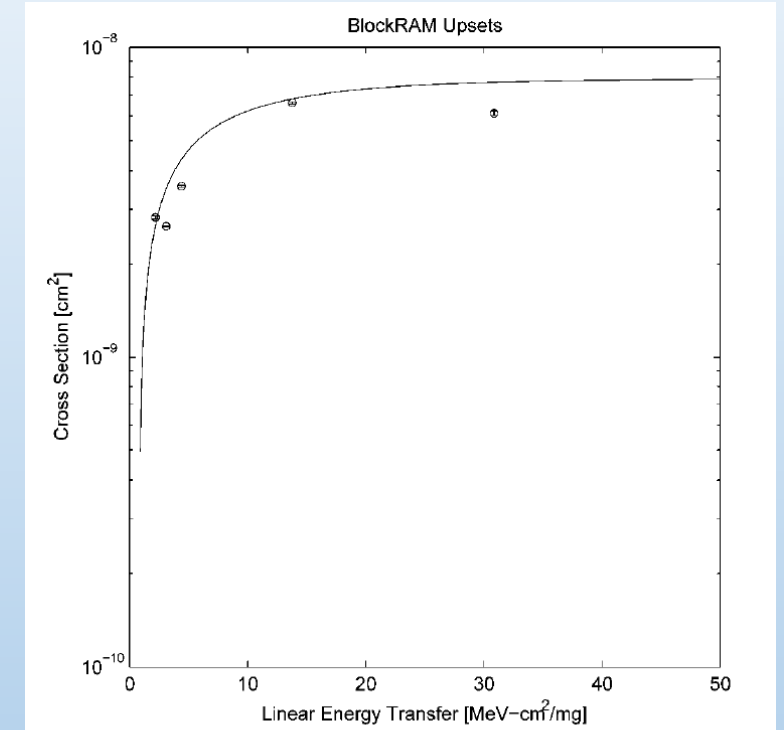
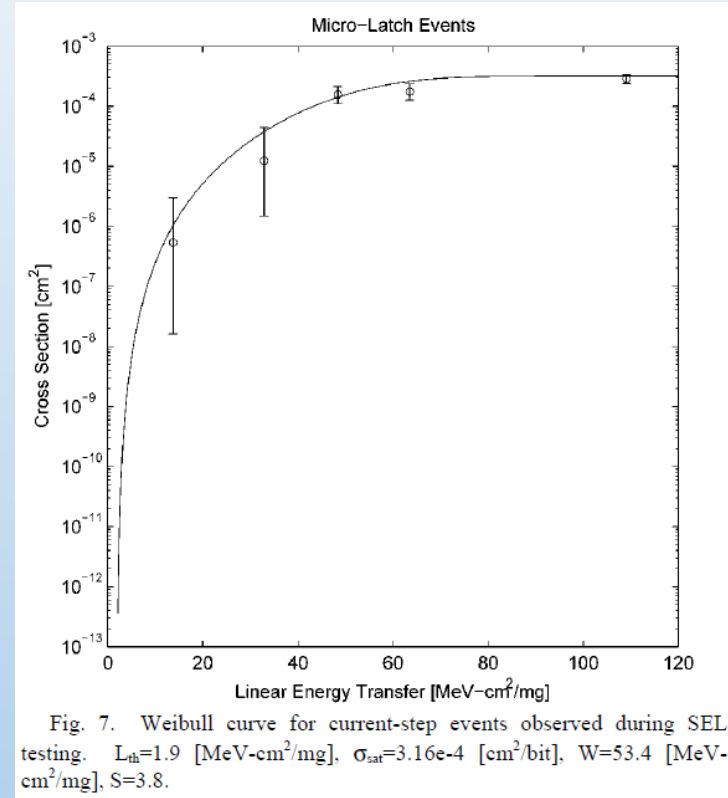
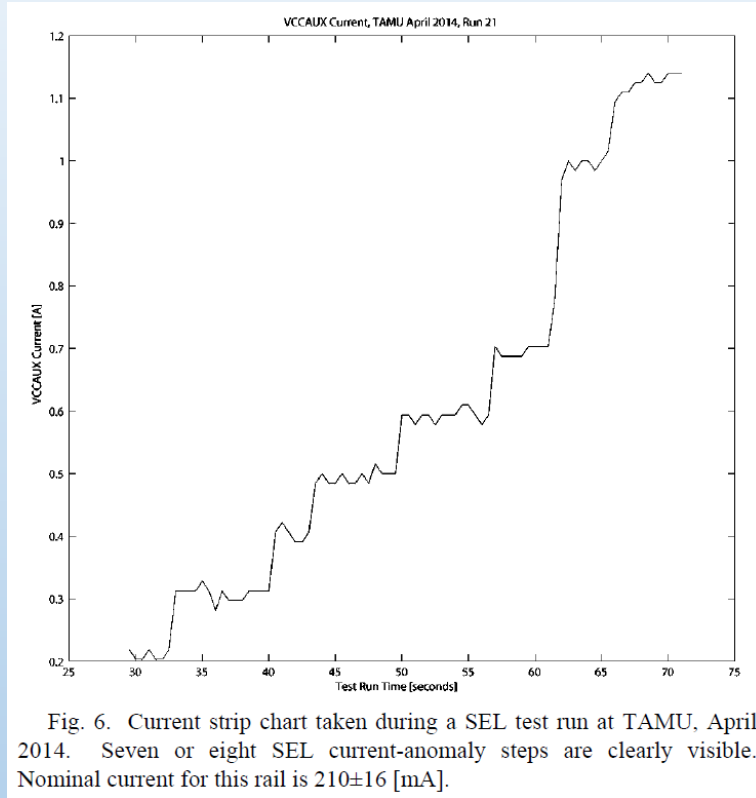


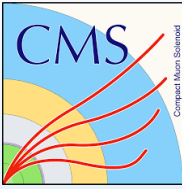
Fig. 5. BlockRAM SEU Weibull curve.  $L_{th}=0.8$  [MeV-cm<sup>2</sup>/mg],  $\sigma_{sat}=7.94e-9$  [cm<sup>2</sup>/bit],  $W=5.0$  [MeV-cm<sup>2</sup>/mg],  $S=0.7$ .

**Mitigation Technique:**  
ECC

# SEL – Kintex7



**Mitigation Technique:**  
**RESET, Flash-reloading,**  
**Power recycling**



# Test facilities and domain of application



- **SEE characterization** of devices requires real-time testing under exposure (functional testing mainly), and the use of particle accelerators,
- **TiD assessment** implies the full parametrical characterization at different step of dose levels received (sequence of irradiation/testing phases). Mostly,  $^{60}\text{Co}$  sources are used for irradiating
- **DD testing** is quite similar to TiD characterization as parametrical measurements and functional checking occurs at different received fluence levels (leading to an equivalent displacement damage dose - DDD6). However, DD testing requires the use of particle accelerators

Standards	Effect	Parameters of concern
ESA-SCC 22900.4	TID	Total dose, dose rate
MIL-STD 883E Method 1019.6	TID	Total dose, dose rate
ESA-SCC 25100.1	SEE	LET/range (heavy ions), Energy (protons)
JESD57	SEE	LET/range (heavy ions)
ESA-SCC 22900.4	DD	Energy

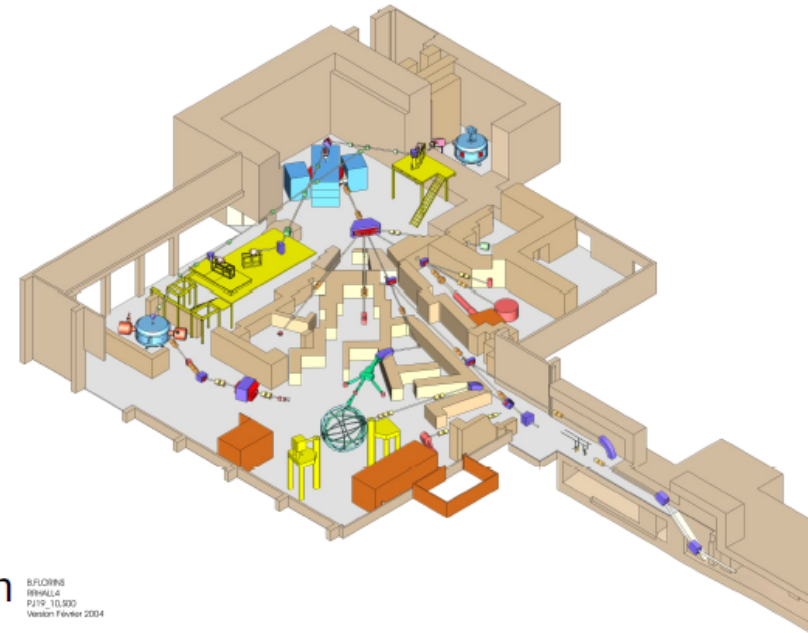
# CRC facilities at Louvain-la-Neuve

Located at Louvain-la-Neuve ( $\sim 20$  km from Brussels)

Institut de Recherche en Mathématique et Physique (IRMP)  
Center for Cosmology, Particle Physics and Phenomenology (CP3)  
Centre de Ressources du Cyclotron (CRC)

Three irradiation facilities

- NIF: Neutron Irradiation Facility
  - ▶ Fast Neutrons (0-50 MeV)
  - ▶ Flux:  $10^{11} \text{ n}/(\text{cm}^2 \text{ s})$
- LIF: Proton Irradiation Facility
  - ▶ Protons 10-60 MeV
  - ▶ Flux:  $5 \times 10^8 \text{ p}/(\text{cm}^2 \text{ s})$
- HIF: Heavy-Ion Irradiation Facility
  - ▶ Heavy Ion "cocktails"
  - ▶ Electronic failures induced by radiation (Single Event Effects)



## HIF characteristics

- Two heavy ions "cocktails" covering a wide range of LET and ranges.
  - ▶ Fully characterisation of SEE response of electronic components.
  - ▶ Fast ion changing within the same cocktail (few minutes)
- Beam flux is variable between a few ions/s.cm<sup>2</sup> and  $\sim 10^4$  ions/s.cm<sup>2</sup>
  - ▶ Can be modified from user station
  - ▶ Online monitoring → high precision in fluence delivered
- Redundant metrology
  - ▶ Fluence and energy
  - ▶ Moving frame, alignment system
  - ▶ ESA SEU monitor: 4x4 Mbit SRAM (Atmel AT60142F) arranged in a square region of 24mm x 24mm
- Beam homogeneity of 10% on a 25 mm diameter.
- Standard mechanical interface and feedthroughs
- Irradiations are done in vacuum and for most of the ions naked chips are needed.



# Heavy Ion Cocktails

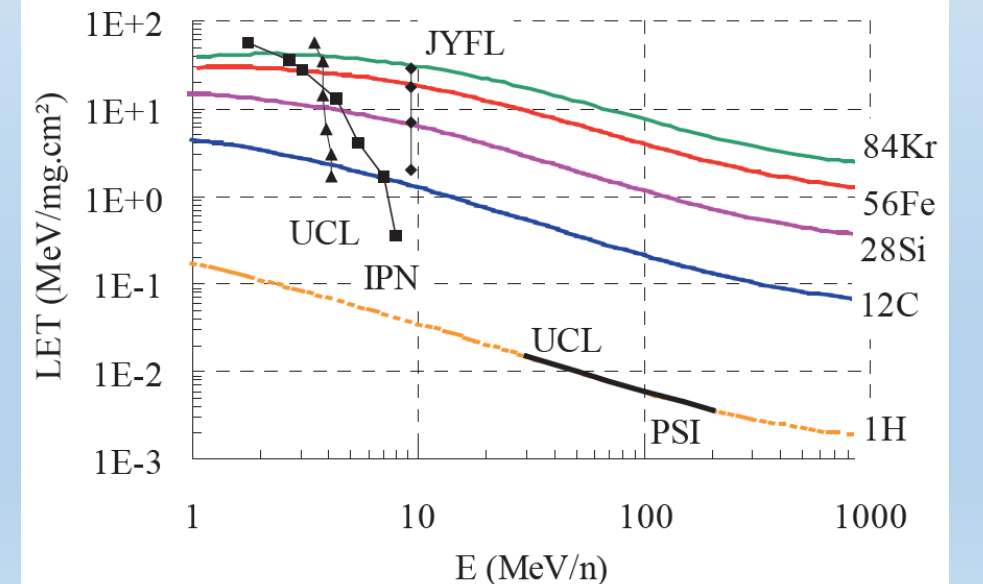
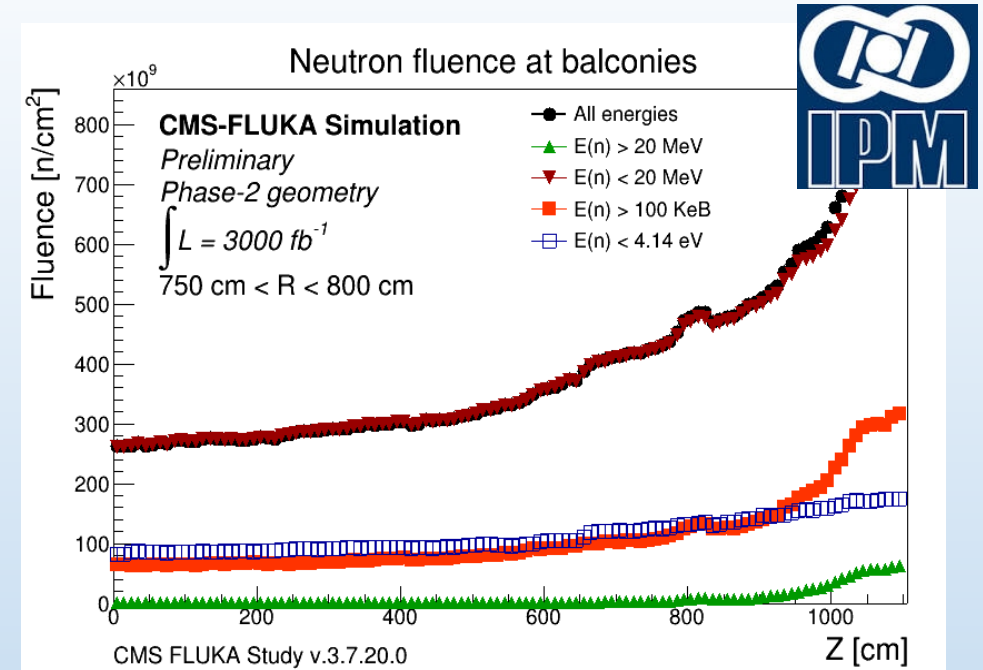
## HIF "cocktails"

Cocktail 1  
High LET

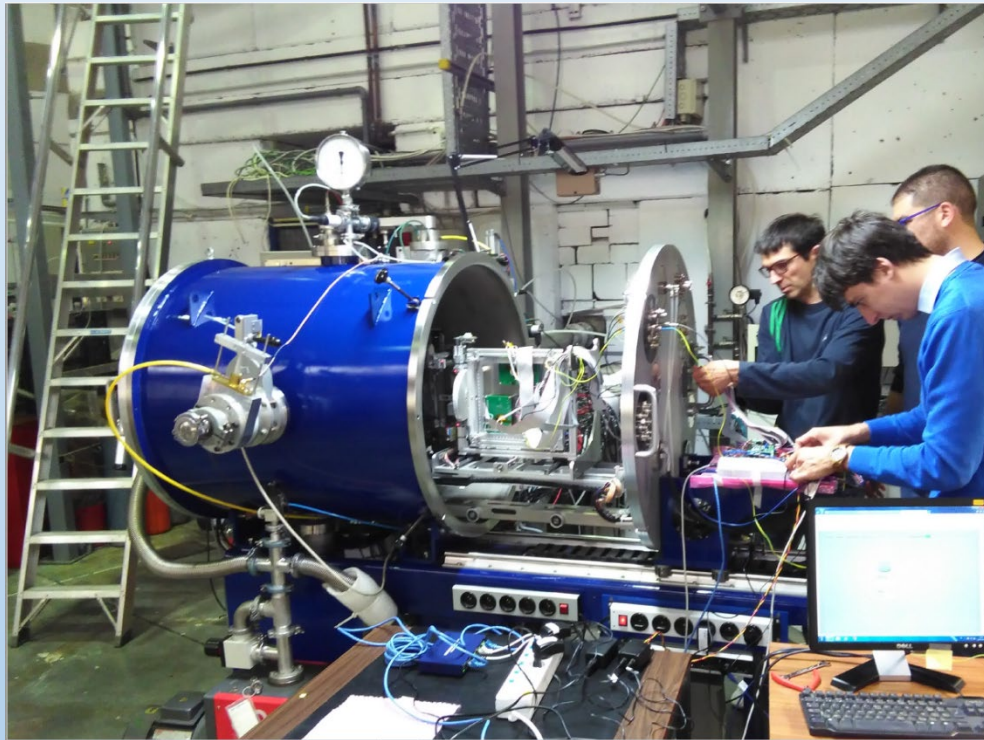
M/Q	Ion	DUT energy [MeV]	Range [ $\mu\text{m Si}$ ]	LET [MeV/mg/cm <sup>2</sup> ]
5	<sup>15</sup> N <sup>3+</sup>	60	59	3.3
5	<sup>20</sup> Ne <sup>4+</sup>	78	45	6.4
5	<sup>40</sup> Ar <sup>8+</sup>	151	40	15.9
4.94	<sup>84</sup> Kr <sup>17+</sup>	305	39	40.4
4.96	<sup>124</sup> Xe <sup>25+</sup>	420	37	67.7

Cocktail 2  
High penetration

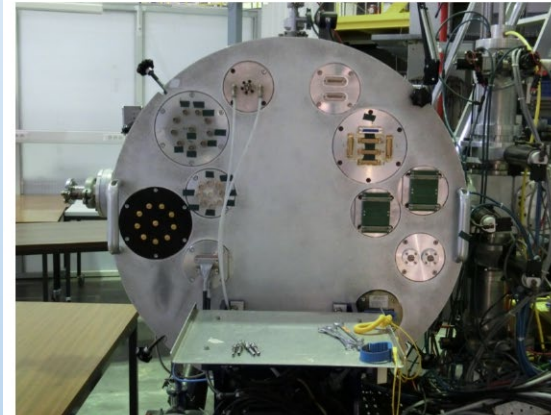
3.25	<sup>13</sup> C <sup>4+</sup>	131	292	1.1
3.14	<sup>22</sup> Ne <sup>7+</sup>	235	216	3
3.33	<sup>40</sup> Ar <sup>12+</sup>	372	117	10.2
3.22	<sup>58</sup> Ni <sup>18+</sup>	567	100	20.4
3.32	<sup>83</sup> Kr <sup>25+</sup>	756	92	32.6
3.54	<sup>124</sup> Xe <sup>35+</sup>	995	73	62.5



# HIF: Heavy Ion Facility UCLouvain Irradiation Test Facility



## Feedthroughs



### Small Flange:

- 8x BNC + 2x SHV (F/F)
- 9x BNC (F/F)
- 2x USB
- 10x SMA (F/F)
- 2x Sub D 25 (M/M)
- 2x HE 10 40 pin (M/M)
- 2x H80A2CO 40 (M/M)
- Water cooling 4-6mm hose with rack connectors input/output + Thermocouple connector

### Large Flange:

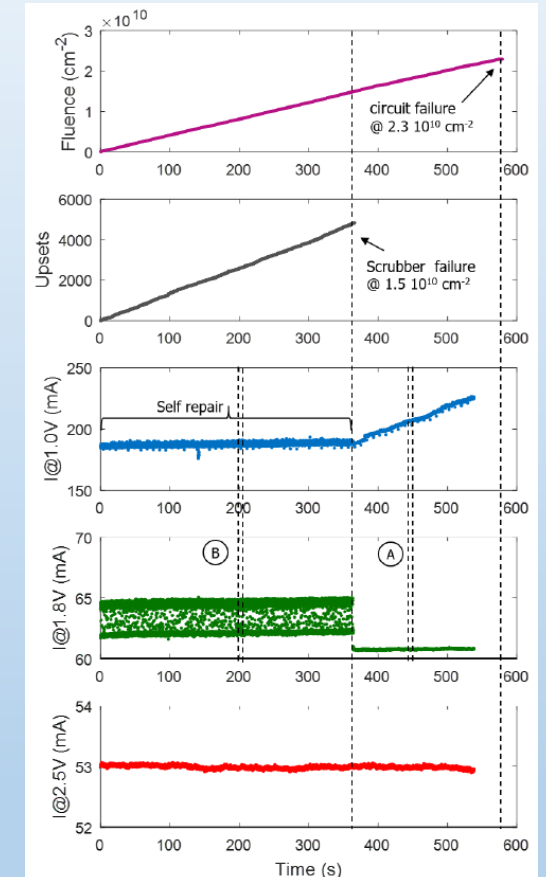
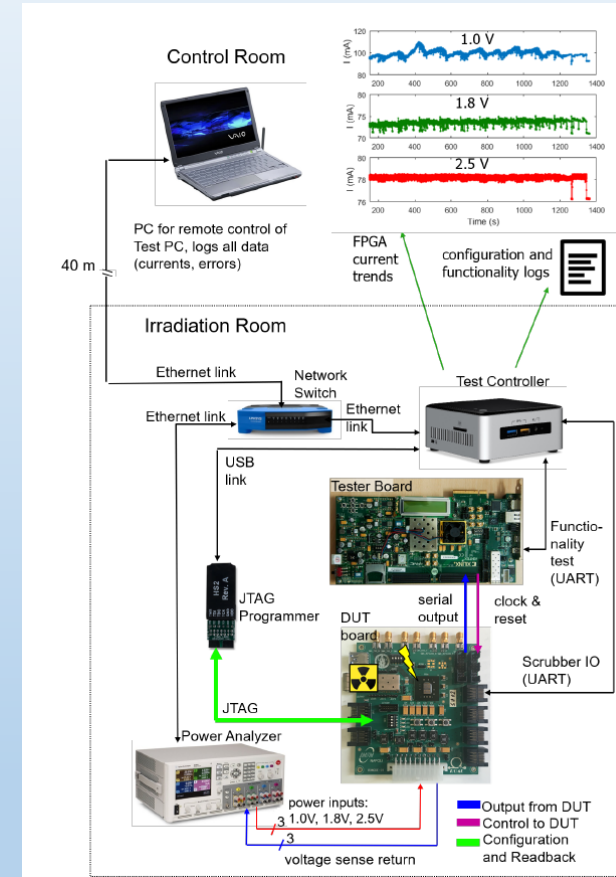
- 10x BNC (F/F)
- 10x BNC ( Ground isolated) (F/F)
- 10x SMA (Ground isolated) (F/F)
- 6x Sub D 25 (Cannot be dismantled) (M outside/F inside)

### Transition available on request:

- Sub-D25 transition to Ethernet (M/Eth, F/Eth)
- USB transition

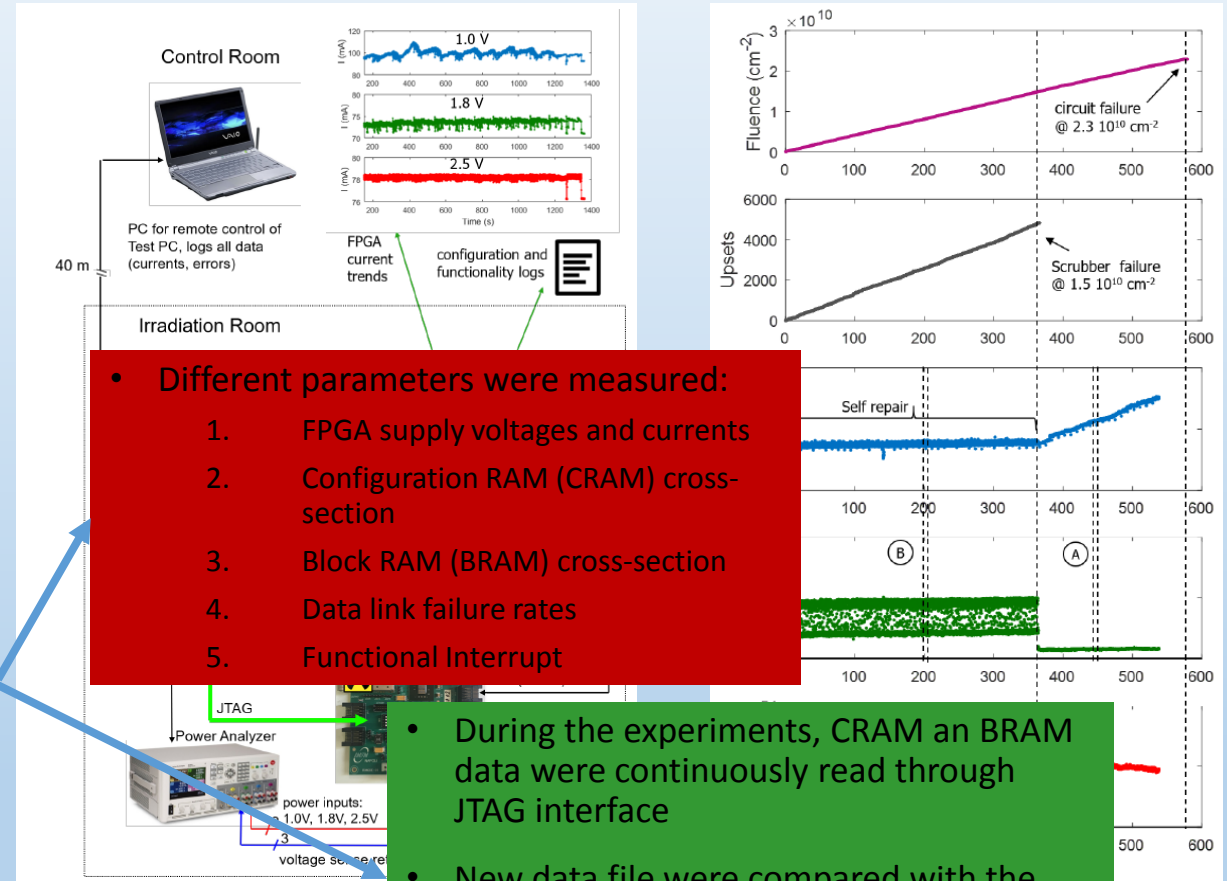
# SEE Test run Sequence

- We measured the impact of the scrubbing core on the reliability of the benchmark design implementations in its different versions (plain and distributed TMR), corresponding to a total of five different firmwares.
- The total irradiation fluence  $800 \times 10^9 \text{ cm}^{-2}$
- Average fluxes per run ranged from  $2.2 \times 10^7 \text{ cm}^{-2} \text{ s}^{-1}$  to  $3.5 \times 10^7 \text{ cm}^{-2} \text{ s}^{-1}$
- Each test run consisted of the following steps
  - power on FPGA
  - configure the FPGA with the redundant bitstream
  - read back configuration
  - activate the scrubber
  - start irradiation
  - wait until the benchmark circuit fails permanently and log if the scrubber fails in the meanwhile
  - stop irradiation
  - verify FPGA configuration against the read back of step 3
  - power off FPGA.



# Test run Sequence

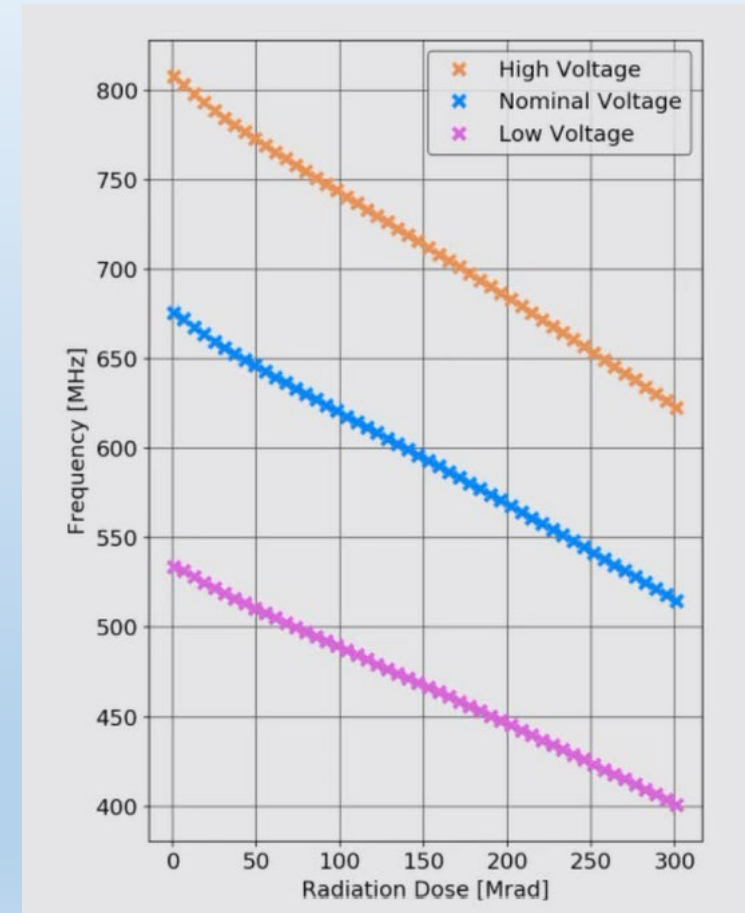
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- Each test run consisted of the following steps
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  - configure the FPGA with the redundant bitstream;
  - read back configuration;
  - activate the scrubber;
  - start irradiation;
  - wait until the benchmark circuit fails permanently and log if the scrubber fails in the meanwhile;
  - stop irradiation;
  - verify FPGA configuration against the read back of step 3;
  - power off FPGA.

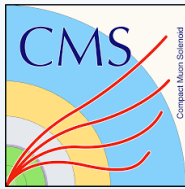


- Different parameters were measured:
  - FPGA supply voltages and currents
  - Configuration RAM (CRAM) cross-section
  - Block RAM (BRAM) cross-section
  - Data link failure rates
  - Functional Interrupt

- During the experiments, CRAM and BRAM data were continuously read through JTAG interface
- New data files were compared with the previous data file and the number of differences between the two files were recorded.

# TID testing with X-Ray





# Radiation Tests Plan for Feb and Link Board



**Neutron Fluence for 10 HL-LHC years is  $1 \times 10^{12} \text{ cm}^{-2}$**   
**Total Integration dose (TID) up to 20 Gy**

Tests to be started:  
Q3 2021 (depending on facility availability)

## Tests for SEE estimation and TID ageing studies:

- **SEE:** Proton and/or Heavy Ions of about 30 - 75 MeV
- **SEE:** Collimated Neutron beam around 25 to 70 MeV
- **TID:** Photons from Cobalt-60 (1 MeV)

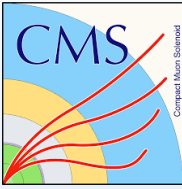
## Facilities:

- **EC Louvain Irradiation Facility**  
both heavy ion and neutron facility (HIF and NIM)
- **Enea Frascati (Rome):** HOTNES (thermal neutron source) + FNG (14 MeV or 2.5 MeV neutrons) + Protons  $\approx$  27 MeV
- **Enea Calliope (Rome):** Co-60 gamma source
- **Cern X-Ray and/or charm facility** to be contacted  
There are 2 Co-60 X-ray facilities, Callab and CC60  
[Irradiation-facilities.web.cern.ch](http://Irradiation-facilities.web.cern.ch)

Main Option

Excellent Plan B, tests could be arranged in few months

Plan C, on site but limited to photons



# Summary



- Radiation Effects on Electronics
- Tests Standards and Guidelines
- Electronics Validation Strategy
- Goals
- How measure the Single Event Effects
- Which type of beam?
  - Proton beam or Heavy Ion
- Where ?
- When, we will ready in Q3 of 2020.
- Plan and Procedure?
- Logistics